MUAD "Harmony" 2M and 1M Ternary CAMs

GENERAL DESCRIPTION

The MUAD "Harmony" Ternary CAM is a fast look-up table device supporting ternary (0, 1, don't care) elements for networking and communication applications. Harmony is a member of MUSIC Semiconductors RouteCAM family.
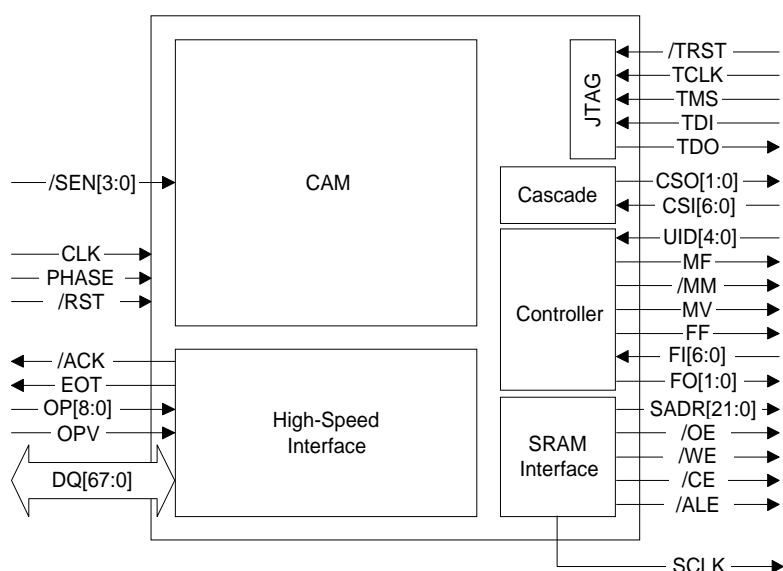
The organization of the Harmony 2M part is 16K x 136 bits, and the 1M part is 8K x 136-bit wide, with double-word and half-word options.

Harmony is ideally suited for high-speed, high-capacity functions, including Ethernet and IP address search, data compression, pattern recognition, cache tags, high-bandwidth address filtering, and fast routing search tables. These functions also include privileged, secured, or encrypted packet-by-packet information utilized in high-performance Internet equipment such as switches, firewalls, bridges, and routers.

The flexibility of the Harmony device allows the creation of multiple search tables within the same device. It compares, simultaneously, the desired information (data) against an entire, pre-stored, array of addresses, providing a performance advantage by reducing search times an order-of-magnitude over typical binary or tree-based search algorithms. The Harmony device can be designed into many applications, but it is particularly well suited to perform highly intensive search operations.

FEATURES

- 16K and 8K x 136-bit full ternary CAMs
- Configurable as 8K/4K x 272 or 32K/16K x 68
- 68-bit interface operates at 13.6Gbit/sec
- Sustains 100 million searches per second on a 68-bit or 136-bit field
- 50 million searches per second in 272-bit configuration
- Holds multiple word widths within the same device
- Synchronous pipelined operation
- Up to eight CAMs cascadable without performance degradation or additional logic
- Glueless interface to industry-standard synchronous SRAMs
- Supports IEEE 1149.1 Test Access
- 1.8 and 3.3V power supply
- 272-pin BGA package

Harmony Block Diagram

CONTENTS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	NC	NC	DQ65	DQ57	DQ53	VDD	VDDQ	DQ43	DQ37	DQ31	VDD	DQ27	DQ21	DQ17	VDD	NC	VDDQ	DQ3	NC	NC
B	NC	VDD	NC	DQ61	NC	DQ49	DQ51	DQ45	VDD	DQ33	DQ29	DQ25	VDDQ	DQ15	DQ13	DQ7	NC	VDD	NC	SADR1
C	TDO	TDI	NC	DQ63	DQ59	DQ55	VDDQ	NC	DQ39	DQ35	NC	DQ23	DQ19	NC	DQ11	DQ5	NC	SADR0	SADR3	SADR2
D	UID0	TMS	TCK	GND	DQ67	VDDQ	DQ47	GND	DQ41	VDDQ	VDDQ	NC	GND	VDDQ	DQ9	DQ1	GND	NC	SADR4	VDDQ
E	UID2	UID3	UID1	/TRST													VDDQ	SADR6	NC	SADR8
F	VDD	CSI2	CSI0	UID4													SADR5	SADR7	SADR11	VDD
G	NC	CSI3	VDDQ	CSI1													VDDQ	SADR9	SADR10	SADR13
H	CSI6	CSI5	CSI4	GND													GND	SADR12	NC	SADR14
J	BHI0	VDDQ	CSO1	CSO0					GND	GND	GND	GND					SADR15	SADR16	VDDQ	SADR17
K	VDD	BHI2	VDD	BHI1					GND	GND	GND	GND					VDD	SADR18	SADR19	SADR20
L	BHO0	BHO1	BHO2	FI0					GND	GND	GND	GND					CLK	SADR21	VDDQ	VDD
M	FI1	FI2	VDDQ	FI3					GND	GND	GND	GND					/WE	/OE	PHASE	SCLK
N	FI4	FI6	NC	GND													GND	/ALE	VDDQ	/CE
P	FI5	NC	NC	FO0													OP2	OP0	OPV	NC
R	VDD	FO1	VDDQ	NC													OP4	OP3	OP1	VDD
T	NC	NC	VDD	/RST													NC	OP6	OP5	VDDQ
U	NC	FF	VDDQ	GND	DQ66	DQ58	DQ54	GND	DQ44	DQ38	DQ30	DQ26	GND	VDDQ	DQ6	DQ0	GND	MF	MV	OP7
V	EOT	/ACK	/SEN3	VDD	/SEN2	DQ56	DQ52	DQ48	VDDQ	DQ36	DQ32	VDDQ	DQ20	DQ14	VDDQ	DQ8	VDDQ	VDD	/MM	OP8
W	GND	NC	/SEN1	/SEN0	VDDQ	NC	VDDQ	DQ46	DQ42	NC	DQ34	DQ28	VDD	DQ16	DQ18	DQ12	NC	DQ4	NC	NC
Y	NC	NC	DQ64	DQ62	DQ60	VDD	DQ50	NC	DQ40	VDD	VDDQ	NC	DQ24	DQ22	VDD	NC	DQ10	DQ2	NC	NC

Figure 1: Connection Diagram

BALL DESCRIPTIONS

This section lists and describes the Harmony signals.

Table 1: MUAD Harmony Ball Descriptions

Symbol	Type	Description	Pin Number(s)
Clocks and Reset			
CLK	I	**Master Clock**. Harmony samples all the control and data signals either on the positive edge of CLK, or on the positive of CLK when PHASE is low.	L17
PHASE	I	**PHASE**. This signal runs at half the frequency of CLK and generates an internal clock from CLK.	M19
SCLK	O	**SRAM Clock**. This signal generates clock for the external SRAM bus. It runs at half the speed of the input CLK.	M20
/RST	I	**Reset**. Driving /RST low initializes the device to a known state.	T4
Instruction and DQ Bus			
OP[8:0]	I	**Instruction Bus**. OP[1:0] specify the instruction. OP[8:2] contain the instruction parameters. The descriptions of individual instructions explain the details of the parameters. The encoding of instructions based on the [1:0] fields are: 00:READ 01:WRITE 10:SEARCH 11:WRITE NEXT FREE ADDRESS	B0:P18, B1:R19, B2:P17, B3:R18, B4:R17, B5:T19, B6:T18, B7:U20, B8:V20
OPV	I	**Op Code Valid**. OPV qualifies the Instruction bus. 0:No Instruction, 1:Instruction	P19
DQ[67:0]	I/O	**Address/Data Bus**. DQ[67:0] carries the read and write address and data during register, data, and mask array operations. It carries the compare data during search operations. It also carries the SRAM address during SRAM accesses.	B0:U16, B1:D16, B2:Y18, B3:A18, B4:W18, B5:C16, B6:U15, B7:B16, B8:V16, B9:D15, B10:Y17, B11:C15, B12:W16, B13:B15, B14:V14, B15:B14, B16:W14, B17:A14, B18:W15, B19:C13, B20:V13, B21:A13, B22:Y14, B23:C12, B24:Y13, B25:B12, B26:U12, B27:A12, B28:W12, B29:B11, B30:U11, B31:A10, B32:V11, B33:B10, B34:W11, B35:C10, B36:V10, B37:A9, B38:U10, B39:C9, B40:Y9, B41:D9, B42:W9, B43:A8, B44:U9, B45:B8, B46:W8, B47:D7, B48:V8, B49:B6, B50:Y7, B51:B7, B52:V7, B53:A5, B54:U7, B55:C6, B56:V6, B57:A4, B58:U6, B59:C5, B60:Y5, B61:B4, B62:Y4, B63:C4, B64:Y3, B65:A3, B66:U5, B67:D5
/ACK	T	**Read Acknowledge**. /ACK indicates that valid data is available on the DQ bus during register, data word, and word mask array READ operations, or the data is available on the SRAM data bus during SRAM READ operations.	V2
EOT	T	**End of Transfer**. EOT indicates the end of burst transfer during READ or WRITE burst operations.	V1
MF	T	**Match Flag**. When asserted, MF indicates that the device is selected in a SEARCH operation.	U18
MV	T	**Match Flag Valid**. When asserted, MV qualifies the Match Flag and Multi-Match Flag signals.	U19
/MM	T	**Multi-Match Flag**. When asserted, indicates that two or more matches were found.	V19
/SEN[3:0]	I	**Search Enable**. /SEN[3:0] controls which pages within the CAM array participate in SEARCH operations. These pins have pull-down resistors, so they may be left unconnected.	B0:W4, B1:W3, B2:V5, B3:V3
SRAM Interface			
SADR[21:0]	T	**SRAM Address**. SADR contains address lines to access external SRAMs that contains associative data. See Tables 22 and 23 for SRAM bus addressing details.	B0:C18, B1:B20, B2:C20, B3:C19, B4:D19, B5:F17, B6:E18, B7:F18, B8:E20, B9:G18, B10:G19, B11:F19, B12:H18, B13:G20, B14:H20, B15:J17, B16:J18, B17:J20, B18:K18, B19:K19, B20:K20, B21:L18
/CE	T	**SRAM Chip Enable**. /CE is the chip enable control for external SRAMs.	N20
/WE	T	**SRAM Write Enable**. /WE is the write enable control for external SRAMs.	M17
/OE	T	**SRAM Output Enable**. /OE is the output enable control for external SRAMs.	M18
/ALE	T	**Address Latch Enable**. /ALE is the latch enable control for external SRAMs.	N18

Table 1: MUAD Harmony Ball Descriptions

Symbol	Type	Description	Pin Number(s)
Cascade Interface			
CSI[6:0]	I	**Cascade In**. These pins depth-cascade the device to form a larger table size. One signal of this bus is connected to the CSO[1] or CSO[0] of each of the upstream devices in a block. Connect all unused CSI pins to a logic 0. For more information, see the Depth-Cascading section.	B0:F3, B1:G4, B2:F2, B3:G2, B4:H3, B5:H2, B6:H1
CSO[1:0]	O	**Cascade Out**. CSO[1] and CSO[0] are the same logical signal. CSO[1] or CSO[0] is connected to one input of the CSI bus of up to four down- stream devices (in a block that contains up to eight devices).	B0:J4, B1:J3
FI[6:0]	I	**Full In**. Each signal in this bus is connected to FO[0] or FO[1] of an upstream device to generate the FF signal for the depth-cascaded block. Connect all unused FI signals to logic 1.	B0:R2, B1:M1, B3:M4, B4:N1, B5:P1, B6:N2
FO[1:0]	O	**Full Out**. FO[1] and FO[0] are the same logical signal. One of these two signals must be connected to the FI of up to four down-stream devices in a depth-cascaded table. Bit[0] in the CAM array indicates if the entry is full (1) or empty (0).This signal is asserted if all bits in the CAM array are 1s.	B0:P4, B1:R2
BHI[2:0]	I	**Block Hit In**. These pins are used for cascading more than eight devices. They must be tied to GND if cascading eight or less devices.	B0:J1, B1:K4, B2:K2
BHO[2:0]	O	**Block Hit Out**. These pins are used for cascading more that eight devices. Output is NC if cascading eight or less devices.	B0:L1, B1:L2, B2:L3
FF	O	**Full Flag**. When asserted, this signal indicates that the table consisting of all depth-cascaded devices is full.	U2
Device Identification			
UID[3:0]	I	**Device Identification**. The binary-encoded device ID for a depth-cascaded system starts at 0000 and goes up to 0111. 1111 is reserved for a special broadcast address that selects all cascaded CAMs in the system. On a broadcast read-only, the device with the LCAM bit set to 1 responds.	B0:D1, B1:E3, B2:E1, B3:E2
UID[4]	I	This device independent bit should be tied to VDD.	F4
Test Access Port Pins			
TDI	I	**Test Data In**	C2
TCK	I	**Test Clock**	D3
TDO	T	**Test Data Out**	C1
TMS	I	**Test Mode Select**	D2
/TRST	I	**Reset**	E4

Note: The BHI and BHO pins would be used when a group of more than eight devices are cascaded; otherwise, these pins are not connected or tied to ground.

FUNCTIONAL DESCRIPTION

The Content Addressable Memory (CAM), High Speed I/O Interface, Cascade Control, SRAM Interface, Test Assess Port, and the Instruction and DQ Bus Interface comprise the Harmony block diagram.

Content Addressable Memory

The CAM section of the Harmony 2M consists of 16,384 136-element ternary words, and the Harmony 1M consists of 8,192 136-element ternary words, arranged such that each ternary element contains a data bit and a mask bit. The combination of data and mask bits determine whether the ternary element address is a 0, 1, or X (don't care). Internally, bit 0 determines if the ternary word contains valid data; if the bit is set to 0, then the word is available as it does not contain valid data. This bit is used to determine the next free address in the device.

The priority encoder generates the address of the word with the lowest address that satisfies the match criteria using the searched data words, CAM array words, and the specified global mask register.

The I/O Interface

The high-speed input port is a double-data rate, 68-bit, data bus incorporated with 9-bits to encode instructions, such as READ and WRITE. The inputs are read on the rising edge of clock, whereas the phase input is used to distinguish between the first and second halves of the I/O cycle. The first half of the I/O cycle transports bits 135:68 and the second half transports bits 67:0.

SRAM Interface

The SRAM interface sections drives the address and control signals required to access the external SRAM. Harmony can generate a synchronous output clock (SCLK) to perform SRAM accesses. Using the SCLK signal Harmony reduces the amount of required interface logic by synchronously driving the SRAM address and control signals. When cascaded, the Harmony device which contains a match in its Results register will drive the SRAM bus. However, in the case where a no match exists, the last Harmony device of the cascade (LRAM = 1) will drive the SRAM bus. Also, when cascaded, this section also inserts pipeline delays for the SRAM address and SRAM control for Harmony. The SRAM data bus is connected to the appropriate host ASIC, therefore SRAM data does not pass through Harmony.

SRAM Addressing

The SRAM address is formed by the information obtained from the DQ bus and either the lowest match address from a SEARCH instruction or the address supplied by Instruction register. The interface timing and control will select the address from the instruction register by asserting the applicable READ or WRITE instruction. During a READ or WRITE instruction to the SRAM, if the identification (UID) is the global address, then the last CAM on the SRAM bus of the depth cascaded devices will drive the SRAM signals (LCAM = 1).

Instruction Bus and DQ Bus

OP[8:0] transports the instruction and its associated parameters. DQ[67:0] is used for data transfer to, and from, the CAM array. The DQ bus transports the search data during the SEARCH instruction as well as the addressing and data during the READ/WRITE operations of the CAM array, and internal registers. The DQ bus also carries the address information for SRAM accesses.

Dual Data Rate Clock

The dual data rate clock, configured as cycle A and cycle B, allows the DQ bus interface to operate at double speed while maintaining 100 Mhz search rates even though the I/O width is less than the data width. Hence, only 68 pins, instead of 136 pins, are required to support 136-bit data words. Furthermore, Harmony can perform consecutive searches on 136-bit data words. The phase signal ensures that these double-speed operations are correctly aligned with Harmony.

Cascade Control

The cascade control section drives the cascade output (CSO) signal when the Harmony devices are depth cascaded. Up to eight Harmony devices can be depth-cascaded. Harmony also contains the control logic to determine if the entry in a single device is full or if the table consisting of multiple devices is full. In addition, the cascade control section provides support for multiple matches. Although the cascade control section does not drive the validity of matches, the success of matches, multiple matches, or the required SRAM signals (these signals are located in the controller section of the block diagram), it does contain the control logic to enable the output for these signals.

Power Management

The power management feature within Harmony reduces power dissipation by limiting search operations to selected portions with the CAM. If known beforehand, the desired data can be isolated and only those portions will need to be selected for the SEARCH instruction. The input pins (/SEN[3:0]) independently control four equal sections of the device. If fewer sections are desired then the designer can connect multiple inputs together. To disable power management, set bit 0 of the Configuration register or connect /SEN[3:0] to GND.

Test Access Port

The Harmony test access port provides an interface for manufacturing tests and consists of the boundary scan access port used to support the standard JTAG IEEE 1149.1.

Initialization

After a hard or soft reset the device register and internal state machines are place in a known state. However, the contents of the CAM must still be initialized. The minimum required initialization will set bit 0 of each 136-bit CAM word to 0 to indicate that the word does not contain valid data. In addition, the table configuration bits of the Instruction register must be initialized to indicate the width of the each of the four addressable sections.

The last CAM in the table bit (LCAM) of the Instruction register must be set to 1 in the last device of the cascaded block; the LCAM bit must be set to 0 in all other devices. In addition, the last CAM on the SRAM bus (LRAM) must be set to 1 in the last device of the cascaded block; the LRAM must be set to 0 in all other devices.

For single Harmony configurations the table size bit, bits 2 and 3, of the Instruction register should be set to 00 to reduce the latency from five or six to four clock cycles. Finally, the Mask register must be initialized to values that depend upon the specific application.

Note: The Mask registers are initialized to all 0s, which will guarantee a match, when compared with any word, in the device regardless of the data values contained. Latency also needs to be initialized.

Depth-Cascading

The Harmony search engine can depth-cascade up to eight devices. Harmony performs all the necessary arbitration to decide which device drives the SRAM bus, thereby eliminating bus contention. The latency of the searches increases as the table size increases; however, the search rate remains constant.

Figure 2 shows how up to eight devices can cascade to form a 128K x 68, 64K x 136, or 32K x 272 bit table and the interconnection between the devices for depth-cascading. Additionally, the host ASIC must program the table size (TLSZ) field to 01. For each search, if a device determines a local match within the device, it asserts the CSO[1:0] signals.
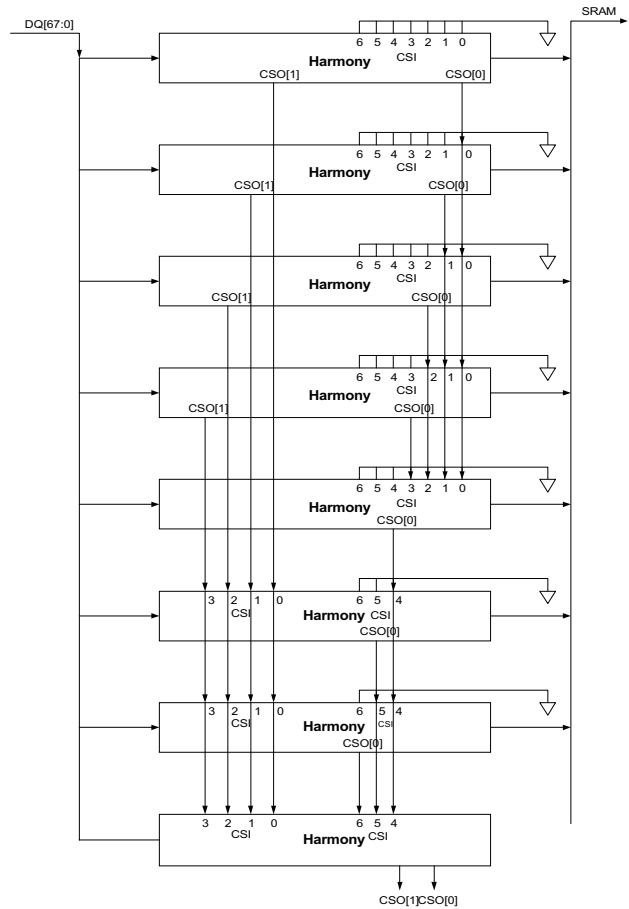
Figure 2: Depth Cascading of Eight Harmony Devices

Arbitration

Four cycles after the SEARCH instruction, each device drives CSO[1:0] with the match result of the search. At the next cycle, all downstream devices know the outcome of the search in all the upstream devices. If any of the upstream devices has a match, all the subsequent devices defer driving the SRAM bus. If a search or no match occurs, Harmony with its LRAM bit set (the last in the chain) drives the SRAM bus signals. Also, the device with LCAM set to 1 is the default driver of the MV, MF, and /MM signals.

Search (68-bit Configuration with LCAM = 1)

The device is configured to be the last in the depth-cascaded table by setting LCAM to 1 in the Instruction register. The device with LCAM set to 1 drives the MV, MF, and /MM signals in cycles when none of the upstream devices drive these signals. Harmony with its LCAM bit set drives MV, MF, and /MM during a search with a no match or with non-search instructions.

Search (68-bit Configuration with LRAM = 1)

The device is configured to be the last on the SRAM bus by setting LRAM to 1 in the Instruction register. In a cycle where the upstream Harmony does not drive the SRAM bus, the last device of the SRAM bus (with LRAM = 1) drives the SRAM control signals (SADR, /CE, /WE, /ALE) when they are active. When set to 1, the LRAM bit sets the default driver for the SRAM control signals (SADR, /CE, /WE, and /ALE).

Depth-Cascading to Generate Full

Bit 0 of each of the entries, regardless of width, is designated as a special bit (1 = Full; 0 = Empty). For each WRITE NEXT FREE ADDRESS or WRITE to the CAM array, a device asserts FO[1] and FO[0] if it does not have any empty locations.The Full Flag (FF) is asserted if the device is full and all FI inputs are high.

Note: The BHI and BHO pins would be used when a group of more than eight devices are cascaded; otherwise, these pins are not connected or tied to ground.
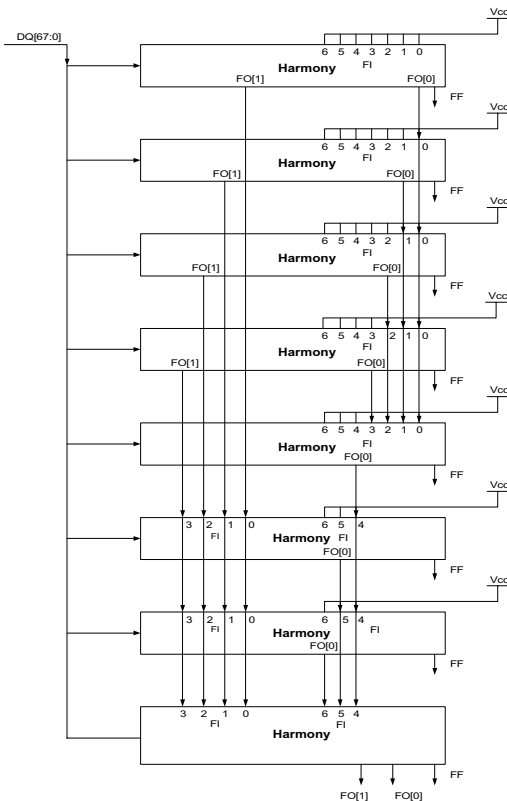

Figure 3: Full Generation in a Cascaded Table

Harmony Table Configuration

The table configuration (CFG) field of the Instruction register allows the designer to configure and manage the internal tables of the Harmony device, using bits 9 through 16. The Harmony (1M) is internally divided into four pages consisting of 2048 x 136 bits, each of which may be configured as 4096 x 68 bits, 2048 x 136 bits, or 1024 x 272 bits by setting the following bits:

- 00:4096 x 68 bits

- 01:2048 x 136 bits

- 10:1024 x 272 bits

Table 2: Table Configuration Bits

Bits	Function
[10:9]	These bits configure the address space within the first quadrant.
[12:11]	These bits configure the address space within the second quadrant.
[14:13]	These bits configure the address space within the third quadrant.
[16:15]	These bits configure the address space within the fourth quadrant.

For the Harmony 2M device, which has a similar architecture, this same bit configuration will yield double the amount of possible entries within the device. For example, setting the bits in the CFG field to 00 would yield a capacity of 8192 x 68 bits as opposed to 4096 x 68 bits.

Multiple Search Table Configuration

There are a variety of ways to internally configure and manage multiple search tables, with variable widths, within the Harmony device. We will show these methods, by example, each of which may be configured by the designer. See Figures 4, 5, and 6.

The Harmony device CAM is divided into four quadrants. Each quadrant may be configured individually to a width of 68 bits, 136 bits, or 272 bits.

The Harmony device is fully capable of performing one-cycle, successive search operations even when configured for half-word widths of 68 bits or two cycle search operations on double-word widths of 272 bits.
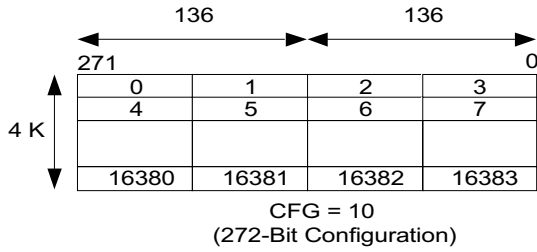
Figure 4: 272-Bit (Double-Word) Configuration

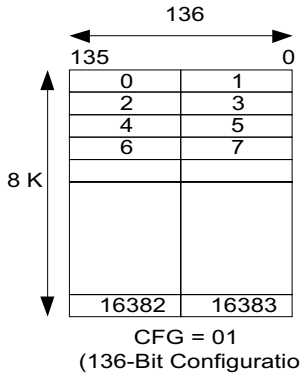*Note: The WRITE NEXT FREE ADDRESS operation is not supported in 272-bit mode.*

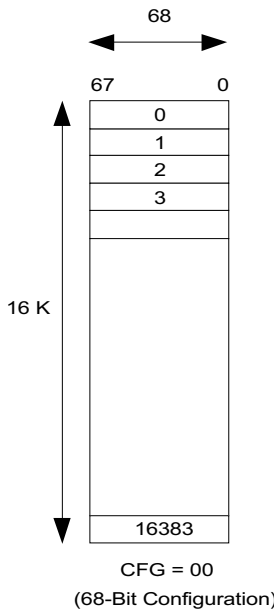**Figure 5: 136-Bit (Single-Word) Configuration**

Figure 6: 68-Bit (Half-Word) Configuration

Multiple Logical Tables of Different Widths

The logical tables in the Harmony device are configured as equal width tables but some applications justify different table widths. The Harmony device may be configured, by quadrant, to support different width logical tables within the same search engine as long as the total number of bits in all combined tables does not exceed the device's maximum

capacity. For example, if the CFG bits [16:9] are set to 10000101 then we will have configured the (2M) device to support four different tables, of widths 2048 x 272 bits, 4096 x 136 bits, 8192 x 68 bits, and 4096 x 136 bits respectively.
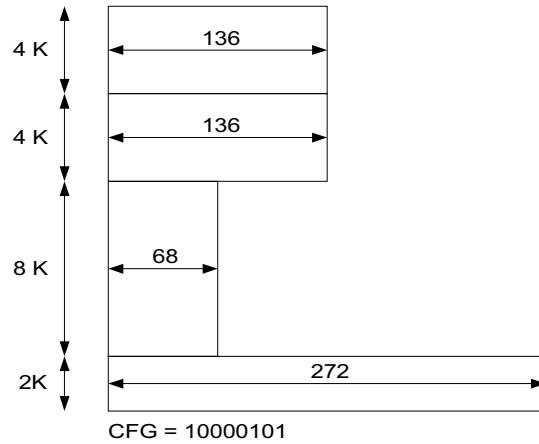
Figure 7: Different Width Example

Depth Cascading to Create Larger Logical Tables

Some high-performance applications require larger tables than can be provided by one device. For these specific applications, up to eight Harmony devices can be depth cascaded to form larger table sizes without a loss of throughput or any external glue logic.

If more than one Harmony is desired, the host ASIC must set the TLSZ field of the Instruction register to 01 and the LCAM (bit 7 in the Instruction register) to 1 in the last Harmony of the depth-cascaded chain. The LCAM bit of all previous devices of the depth-cascaded chain must then be set to 0. Similarly, the last CAM on the SRAM bus (LRAM) signal, bit 8 in the Configuration register, must be set to 1 in the last Harmony of the depth-cascaded chain connected to the SRAM bus. The LRAM bit of the other Harmony devices must then be set to 0.

When the TLSZ field is set to one, the MF, /MM, and MV signals will have five clock cycles of latency. When a single Harmony is used, the TLSZ field of the Instruction register can be set to 0 to reduce the latency from five or six to four clock cycles. Harmony will perform all of the necessary arbitration to decide which device will drive the SRAM bus. Although the latency of the searches will increase proportionally with the table sizes, the search rate will remain constant. For each search, if the device determines a match within the device, then the CSO[1] and CSO[0] signals will be asserted. See Table 24 on page 19 for TLSZ configurations.

REGISTER DESCRIPTIONS

Harmony contains sixteen Comparand registers, the Global Mask register (consisting of nine registers), Result, Instruction, Information, Burst Read, Burst Write, Next Free Address, and Configuration registers. Table 3 provides an overview of the Harmony registers. The registers are ordered in ascending address order. Each register group is described in the following subsections.

Table 3: Register Overview

| Address	Abbreviation	Type	Name
0–31	CMPR[0–31]	R	16 136-bit Comparand Registers. Stores comparands from the DQ bus for writing later.
32–47	GMR[0-7]	R/W	Eight 136-bit Global Mask Registers
48–55	RR[0–7]	R	Eight Result Registers
56	INSTR	R/W	Instruction Register
57	INFO	R	Information Register
58	RBAR	R/W	Burst Read Address Register
59	WBAR	R/W	Burst Write Address Register
60	NFA	R	Next Free Address Register
61	CONFIG	R/W	Configuration Register
62–63	N/A	N/A	Reserved
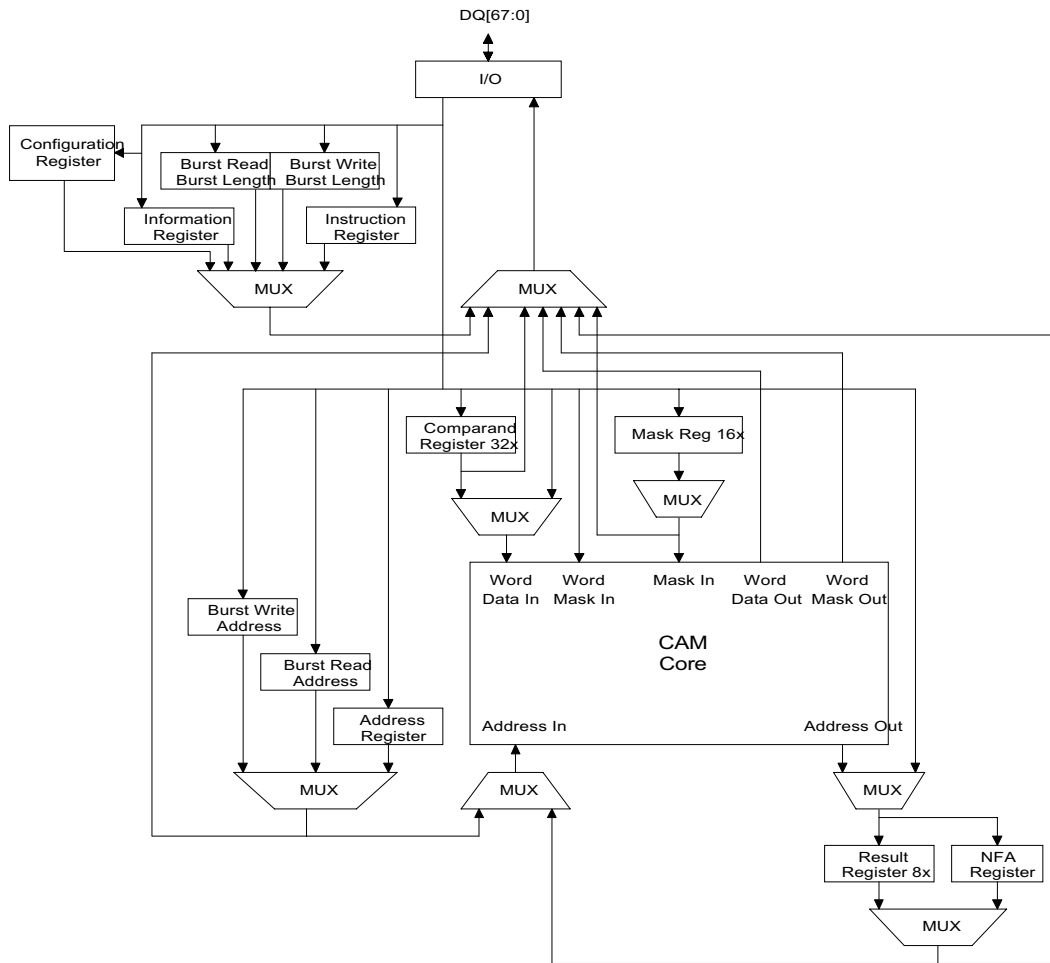
Figure 8: Internal Datapath Diagram of the Harmony Registers

Comparand Registers

The device contains eight 136-bit Comparand registers dynamically selected in every SEARCH operation to store the comparand presented on the DQ bus. These registers will later be used by the WRITE NEXT FREE ADDRESS.

In Cycle A of the SEARCH instruction, Harmony stores the SEARCH data bits[135:68]) in the even-number Comparand register. In Cycle B, Harmony stores the SEARCH data bits[67:0] in the odd-numbered Comparand register. See Figure 9.
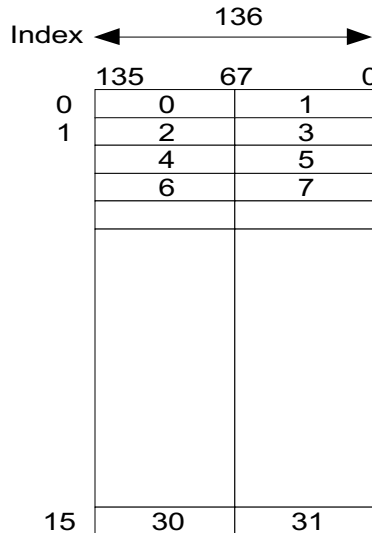
Figure 9: Comparand Registers Address and Usage

Global Mask Registers

The device contains eight 136-bit Global Mask registers dynamically selected in every SEARCH operation to select the search subfield. Figure 10 specifies the address of these registers. The 3-bit global search or write index supplied on the Instruction bus applies eight global masks during the SEARCH and WRITE operations, as shown in Figure 10.

Note: In a 68-bit configuration, the host must program the even and odd mask register with the same value; Harmony uses even-numbered mask registers as global masks.

SEARCH and WRITE Command Global Mask Se

Figure 10: Addressing the Global Mask Register

A mask bit in the Global Mask registers is used during SEARCH and WRITE operations. In SEARCH operations, setting the mask bit to 1 enables compares; setting the mask bit to 0 disables compares (forced match) at the current bit position. In WRITE operations to the data or mask array, setting the mask bit to 1 enables writes; setting the mask bit to 0 disables writes at the current bit position.

During a SEARCH operation, the search data bit (S), data bit (D), mask bit (M) and the global mask bit (G) are used in the following manner to generate a match at that bit position (see Table 4).

Table 4: Bit Position Map

G	M	S	D	Match
0	x	x	x	1
1	0	x	x	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Result Registers

The device contains eight Result registers to hold the lowest match address (LMA) found during a SEARCH operation. The SEARCH instruction specifies which Result register to use by parsing the Result register index in Cycle B of the SEARCH instruction.

Subsequently, the host uses this register to access the mask of the word at the LMA or external SRAM using the index as part of the address (see SRAM Addressing on page 4). The device with a valid bit set performs a READ or WRITE operation. All other devices suppress the operation.

Table 5: Result Register (1M)

Bit(s)	Name	Initial Value	Description
[13:0]	INDEX	x	**Index**. This is the address of the 68-bit entry where a successful search occurs. The device updates this field if it has a successful search. In 136-bit, the LSB is 0; in a 272-bit configuration, the two LSBs are 00.
[30:14]	N/A	0	**Reserved**
[31]	VALID	0	**Valid**. The device sets this bit to 1 if it is a global winner (first Harmony downstream with a hit) in a SEARCH operation.
[67:32]	N/A	0	**Reserved**

Table 6: Result Register (2M)

Bit(s)	Name	Initial Value	Description
[14:0]	INDEX	x	**Index**. This is the address of the 68-bit entry where a successful search occurs. The device updates this field if it has a successful search. In 136-bit, the LSB is 0; in a 272-bit configuration, the two LSBs are 00.
[30:15]	N/A	0	**Reserved**
[31]	VALID	0	**Valid**. The device sets this bit to 1 if it is a global winner (first Harmony downstream with a hit) in a SEARCH operation.
[67:32]	N/A	0	**Reserved**

Instruction Register
Table 7: Instruction Register

Bit(s)	Name	Initial Value	Description
[0]	SRST	0	**Software Reset**. If 1, this bit resets the device with the same effect as a hardware reset. Internally, it generates a reset pulse lasting for eight CLK cycles. This bit automatically resets to a 0 if written with a 1.
[1]	DEVE	0	**Device Enable**. If 0, the device does not perform any SEARCH, WRITE, WRITE NEXT FREE ADDRESS, and READ operations, and it keeps the SRAM bus in 3-state condition, forcing the cascade interface outputs to 0.
[3:2]	TLSZ	01	**Table Size**. The host must program this field to configure the chips into a table of a certain size. This field affects the pipeline latency of the SEARCH and WRITE NEXT FREE ADDRESS operations as well as the accesses to the SRAM (SADR[21:0], /CE, /OE, /WE, /ALE, MV, MF, /MM, and /ACK). Once programmed, the search latency stays constant. **Number of Devices** **CLK** 00:1 device 4 01:2-4 devices 5 10:5-8 devices 6 11:Reserved
[6:4]	RLAT	000	**Latency of Hit Signals**. This field adds latency to the MF, MV, /MM, and /ACK signals by the following number of CLK cycles during SEARCH and SRAM READ operations. 000:0 100:4 001:1 101:5 010:2 110:6 011:3 111:7
[7]	LCAM	0	**Last CAM in Table**. This device is the last CAM in the depth-cascaded table. In the event of a search failure, the device with this bit set drives the hit signals as follows. MF = 0, MV = 1. During non-search cycles, the device with this bit set drives the signals as follows. MF = 0, MV = 0.

Table 7: Instruction Register (continued)

Bit(s)	Name	Initial Value	Description
[8]	LRAM	0	**Last CAM on this SRAM Bus**. This device is the last CAM on this SRAM bus. In cycles where a CAM does not drive the SRAM bus, the device with this bit set drives the SRAM bus (SADR, /CE, and /WE) in their inactive state. This bit sets a default driver for the SRAM control signals (SADR, /CE, /WE, and /OE). *Note: /OE is always asserted or deasserted.*
[16:9]	CFG	10000101	**Table Configuration**. The device is internally divided into four quadrants of 8K x 68, each of which can be configured as 8K x 68, 4K x 136, or 2K x 272 as follows. 00:8K x 68 01:4K x 136 10:2K x 272 11:Reserved Bits[10:9] apply to configuring the 1st quadrant in the address space. Bits[12:11] apply to configuring the 2nd quadrant in the address space. Bits[14:13] apply to configuring the 3rd quadrant in the address space. Bits[16:15] apply to configuring the 4th quadrant in the address space.
[67:17]	N/A	0	**Reserved**

Information Register

Table 8: Information Register

Bit(s)	Name	Initial Value	Description
[11:0]	MFD	000100110011	**Manufacturer ID**. These bits include the JTAG bit LSB = 1.
[27:12]	DEVID	1010110100000010	**Device Identification**. These bits indicate the device identification number.
[31:28]	RVSN	0001	**Revision Number.** This is the current device revision number. This number increments by 1 for each revision of the device.
[67:32]	N/A		**Reserved**

Burst Read Address Register

The Burst Read Address register fields must be programmed before each BURST READ operation.

Table 9: Burst Read Address Register

Bit(s)	Name	Initial Value	Description
[13:0]	ADDR	0	**Address**. This is the starting address of the location of the CAM array during a BURST READ operation. It automatically increments by 1 for each successive READ of the CAM array.
[18:14]	N/A	0	**Reserved**
[27:19]	BLEN	0	**Length of Burst Access**. The device can READ from 4 up to 511 locations in a burst mode. Up to the maximum number of devices, this decrements to back 0.
[67:28]	N/A	0	**Reserved**

Burst Write Address Register

The Burst Write Address register fields must be programmed before BURST WRITE operations.

Table 10: Burst Write Address Register

Bit(s)	Name	Initial Value	Description
[13:0]	AADR	0	**Address**. This is the starting address of the location of the CAM array during a BURST WRITE operation. It automatically increments by 1 for each successive WRITE of the CAM array.
[18:14]	N/A	0	**Reserved**.
[27:19]	BLEN	0	**Length of Burst Access**. The device provides the capability to WRITE from 4 up to 511 locations in a burst mode. Up to the maximum number of devices, this decrements to back 0.
[67:28]	N/A	0	**Reserved**.

Next Free Address Register

Bit 0 of each, regardless of width, entry is a special bit designated for use in the operation of the WRITE NEXT FREE ADDRESS instruction. In 68-bit configurations, bit 0 indicates whether a location is full (bit set to 1) or empty (bit set to 0). Every WRITE and WRITE NEXT FREE ADDRESS instruction loads the address of first 68-bit location that contains a 0 in the entry's bit 0. This is stored in the Next Free Address register. If the bits of the LSB in a device are set to 1, Harmony asserts FO[1:0] to 11. FF should also be set to 1 in each data word.

In 136-bit configuration, the (LSB) of this register is always set to 0. Regardless of the configured word width, the host must set bit 0 of each word to 0 (empty) or 1 (full) to indicate the full/empty status of each entry.

Configuration Register
Table 11: Configuration Register

Bit(s)	Name	Initial Value	Description
[0]	SENE	0	**Enable Search Enable**. When this bit is set to 1, /SEN[3:0] are enabled. These pins are individual quadrant enables. When SENE is set to 0, the /SEN[3:0] pins have no effect.
[1]	MME	0	**Multi-Match Enable**. When this bit is set to 1, the /MM output is enabled. Else, the /MM is disabled (3-state).
[2]	SCE		**SCLK Enable**. When this bit is set to 1, the SCLK output is enabled. Else, the SCLK output is disabled (3-state).
[67:3]	N/A	0	**Reserved**.

HARMONY INSTRUCTIONS

A master device, such as a controller, issues instructions to Harmony using the Op Code Valid (OPV) signal and the Instruction bus. The following subsections describe the functions of the instructions.

Instruction Codes

Harmony implements four basic instructions (see Table 12). OP[1:0] apply the instructions to the device while keeping the command valid (OPV) signal high for two CLK cycles. These two CLK cycles are designated as Cycle A and Cycle B.

The OP[8:2] field passes the parameters of the instruction in Cycles A and B. The controller must align the instructions with the CLK signal.

Table 12: Harmony Instructions

Code	Instruction	Description
00	READ	Reads one of the following: CAM Array, Register locations or external SRAM.
01	WRITE	Writes one of the following: CAM Array, Register locations or external SRAM.
10	SEARCH	Searches the CAM array for a desired pattern using the specified register from the Global Mask register array and local mask associated with each data cell.
11	WRITE NEXT FREE ADDRESS	The device can write up to 16 comparands for internal storage. The device's controller inserts these entries at the next free address (as specified by the NFA register) using the WRITE NEXT FREE ADDRESS instruction.

Instructions and Instruction Parameters

Table 13 lists the Instruction bus fields that contain Harmony instruction parameters and their respective cycles. Each instruction is described separately in subsections following this table.

Table 13: Instruction Parameters

Instruction	Cyc	8	7	6	5	4	3	2	1	0
READ	A	SADR[21][1]	SADR[20][1]	SADR[19][1]	0	0	0	0 = Single 1 = Burst	0	0
	B	0	0	0	0	0	0	0 = Single 1 = Burst	0	0
WRITE	A	SADR[21][1]	SADR[20][1]	SADR[19][1]	Global Mask Register Index			0 = Single 1 = Burst	0	1
	B	0	0	0	Global Mask Register Index			0 = Single 1 = Burst	0	1
SEARCH	A	SADR[21]	SADR[20]	SADR[19]	Global Mask Register Index			68-bit or 136-bit: 0 272-bit: 1 in 1st Cycle 0 in 2nd Cycle	1	0
	B	Result Register Index[2:0]			Comparand Register Index				1	0
WRITE NEXT FREE ADDRESS[2]	A	SADR[21]	SADR[20]	SADR[19]	Comparand Register Index				1	1
	B	0	0	Mode 0:68-bit 1:136-bit	Comparand Register Index				1	1

Notes:

1.   *For SRAM read/write only.*
2.   *The WRITE NEXT FREE ADDRESS instruction is not supported when the table width is 272 bits.*

READ Instruction

The READ instruction, configured as a SINGLE READ (OP[2] = 0) or as a BURST READ (OP[2] = 1), will read the CAM array, synchronous random access memory (SRAM), or register location. The SINGLE READ instruction operates in six clock cycles. However, the BURST READ requires two additional clock cycles for each successive READ instruction. Refer to Tables 14, 15, 16, and 17 for the READ address formats.

SINGLE READ Instruction

During the first cycle, the host ASIC configures the OP[1:0] (OP[2] = 0), using OPV = 1 and applies the READ instruction, while the DQ bus supplies the address. The host selects the device for which UID[4:0] matches the DQ[25:21] lines, or the last chained Harmony of the cascade when DQ[25:21] = 11111. The host ASIC also will supply SADR[21:19] on OP[8:6] in the first cycle of the READ instruction, if the READ has been applied to an external SRAM.

For the next two cycles the host ASIC will hold the DQ[67:0] bus in a 3-stated, high Z mode. Afterwards, in the fourth cycle, the device selected by the host will drive the DQ[67:0] bus and pull the /ACK signal from Z to low. In the fifth cycle, the device selected by the host will drive data to be read from the addressed location on DQ[67:0] and assert the /ACK signal to high.

Lastly, the selected device 3-states DQ[67:0] and deasserts /ACK to low. Upon the termination of the last cycle, the selected device 3-states the /ACK, completes the SINGLE READ instruction, and prepares Harmony for the next instruction.

BURST READ Instruction

The burst length (BLEN) field of the Burst Read Address (RBAR) register determines the latency of the BURST READ instruction. The BURST READ instruction completes in four clock cycles plus twice the number of burst accesses. Note that, before initiating the BURST READ instruction, the host must first program the BURST READ Address register with the start address and the length of transfer. The following sequence delineates the clock cycles required of the BURST READ instruction:

In the first cycle, the host ASIC configures the OP[1:0] (OP[2] = 1), using OPV = 1 and applies the READ instruction, while the DQ bus supplies the address. The host will then select the device for which UID[4:0] matches the DQ[25:21] lines, or the last chained device when DQ[25:21] = 11111. The host will also supply SADR[21:19] on OP[8:6] in first cycle of the BURST READ instruction if the READ instruction has been applied to an external SRAM.

For the next two cycles the host will 3-state (HIGHZ) DQ[67:0]. In the fourth cycle, the device selected by the host will drive DQ[67:0] to signal the end of transfer, and deassert /ACK from Z to low. In the fifth cycle, the selected device (selected by the host) will drive the data to be read from the addressed location on DQ[67:0] and assert /ACK signal back to high. These fourth and fifth cycles are repeated until all of the specified accesses in the burst length (BLEN) field of the Burst Read Address register have been depleted.

On the last transfer, the selected device drives DQ[67:0] to a 3-stated position, asserts the end of transfer (EOT) signal to high and deasserts /ACK to low. Upon the termination of the last cycle, cycle 4 + 2n (where n is the number of burst accesses), the selected device 3-states the /ACK signal, completes the BURST READ instruction, and prepares Harmony for the next instruction.

Table 14: Read Instruction Parameters

Instruction Parameter OP[2]	Read Instruction	Description
0	SINGLE READ	Reads a single location of the CAM array, external SRAM, or device registers. All access information is applied on the DQ bus.
1	BURST READ	Reads a block of locations from the CAM array as a burst. The internal register (RBAR) specifies the starting address and the length of the data transfer from the CAM array, and it auto-increments the address for each access. All other access information is applied on the DQ bus. **Note:** *The device registers and external SRAM can only be read in single-read mode.*

Table 15: CAM or SRAM Read Address Format

DQ [67:30]	DQ [29]	DQ [28:26]	DQ [25:21]	DQ [20]	DQ [19]	DQ [18:14]	DQ [13:0]
Reserved	0:Direct 1:Indirect	Result Register Index (Applicable if DQ[29] is indirect)	UID	0	0:Data 1:Mask	Reserved	If DQ[29] is 0, this field carries address of data location. If DQ[29] is 1, the Result register specified on DQ[28:26] supplies the address of the data location.
Reserved	0:Direct 1:Indirect	Result Register Index (Applicable if DQ[29] is indirect)	UID	1	0	Reserved	If DQ[29] is 0, this field carries address of SRAM's location. If DQ[29] is 1, the Result register specified on DQ[28:26] supplies the address of the SRAM's data location.

Note: DQ[25] should be set to 1.

Table 16: Internal Registers Read Address Format

DQ[67:26]	DQ[25:21]	DQ[20:19]	DQ[18:6]	DQ[5:0]
Reserved	UID	11:Register	Reserved	Register Address

Table 17: CAM Read Address for BURST READ

DQ[67:26]	DQ[25:21]	DQ[20]	DQ[19]	DQ[18:14]	DQ[13:0]
Reserved	UID	0	0:Data 1:Mask	Reserved	Don't Care. These 14 bits come from the internal register (Burst Read Address register) which increments for each access.

WRITE Instruction

The WRITE instruction can be configured for SINGLE WRITE (OP[2] = 0) or BURST WRITE (OP[2] = 1) instruction of a CAM array, register location, or external SRAM locations or using the internal auto-incrementing Burst Write Address register, of the CAM array locations. The SINGLE WRITE instruction can be completed in only three-cycles. However, the BURST WRITE operation requires an additional cycle for each successive WRITE.

SINGLE WRITE Instruction

In the first cycle, the host applies the WRITE instruction on the OP[1:0] (OP[2] = 0), using OPV=1 and the supplied address on the DQ bus. The host will also supply the index to the Global Mask register to mask the WRITE instruction to the CAM array's location in OP[5:3]. For the WRITE instruction, the host selects the device for which UID[4:0] match DQ[25:21] or all connected devices when DQ[25:21] = 11111.

In the second cycle, the host drives DQ[67:0] with the data to be written to the CAM array, external SRAM, or register location of the selected device. The third cycle is an idle cycle, and soon after this idle period the device is ready for the next instruction.

BURST WRITE Instruction

The BURST WRITE instruction operates for the number of burst accesses specified by the burst length (BLEN) field of the Burst Write Address register plus two additional clock cycles. Note that, before initiating the BURST WRITE instruction, the host must program the Burst Write Address register with the start address and the length of transfer as indicated in the BLEN field. The following summarizes the sequence of the BURST WRITE instruction

In the first cycle, the host applies the WRITE instruction on the OP[1:0] (OP[2] = 1), using OPV = 1 and supplied address on the DQ bus. The host also supplies the index to the Global Mask register to mask the WRITE to the CAM array locations in OP[5:3]. The host will then select the device for which UID[4:0] match the DQ[25:21], or all devices when DQ[25:21] = 11111.

In the second cycle, the host drives DQ[67:0] with the data to be written to the CAM array location of the selected device. On DQ[67:0], the host will only write the data to the corresponding subfield that has its mask bit set to 1 in the Global Mask register. This is specified by the index OP[5:3] and supplied in the first cycle.

From the third cycle to number of burst accesses (indicated by the BLEN field) plus one additional access, n^{th} cycle +1, the host drives DQ[67:0] with the data to be written to the CAM array's next location (addressed by the auto-increment address field of the Burst Write Address register).

This is specified by OP[5:3] index and supplied by the first cycle. The host drives the end of transfer signal to low from the third to the nth cycle. Afterward, the host drives this same signal to high one cycle after the nth cycle. This value, n, is specified by the BLEN field of the Burst Write Address register.

Two cycles after the nth cycle, the host will drive the end of transfer signal to low. Afterward, when the cycle terminates, the host drives the end of transfer signal to a Z state, and prepares Harmony for the next instruction.

Table 18: CAM or SRAM (SINGLE WRITE) Write Address Format for 1M Harmony

DQ [67:30]	DQ [29]	DQ [28:26]	DQ [25:21]	DQ [20]	DQ [19]	DQ [18:14]	DQ [13:0]
Reserved	0:Direct 1:Indirect	Result Register Index (Applicable if DQ[29] is indirect)	UID	0	0:Data 1:Mask	Reserved	If DQ[29] is 0, this field carries the address of the data location. If DQ[29] is 1, the Result register specified by DQ[28:26] supplies the address of the data location.
Reserved	0:Direct 1:Indirect	Result Register Index (Applicable if DQ[29] is indirect)	UID	1	0	Reserved	If DQ[29] is 0, this field carries address of the SRAM's location. If DQ[29] is 1, the successful search register specified by DQ[28:26] supplies the address of the SRAM's location.

Table 19: CAM or SRAM (SINGLE WRITE) Write Address Format for 2M Harmony

DQ [67:30]	DQ [29]	DQ [28:26]	DQ [25:21]	DQ [20]	DQ [19]	DQ [18:15]	DQ [14:0]
Reserved	0:Direct 1:Indirect	Result Register Index (Applicable if DQ[29] is indirect)	UID	0	0:Data 1:Mask	Reserved	If DQ[29] is 0, this field carries the address of the data location. If DQ[29] is 1, the Result register specified by DQ[28:26] supplies the address of the data location.
Reserved	0:Direct 1:Indirect	Result Register Index (Applicable if DQ[29] is indirect)	UID	1	0	Reserved	If DQ[29] is 0, this field carries address of the SRAM's location. If DQ[29] is 1, the Result register specified by DQ[28:26] supplies the address of the SRAM's location.

Table 20: Internal Registers Write Address Format

DQ[67:26]	DQ[25:21]	DQ[20:19]	DQ[18:6]	DQ[5:0]
Reserved	UID	11:Register	Reserved	Register Address

Table 21: CAM (BURST WRITE) Write Address Format

DQ [67:26]	DQ [25:21]	DQ [20]	DQ [19]	DQ [18:14]	DQ [13:0]
Reserved	UID	0	0:Data 1:Mask	Reserved	Don't care. These 14 bits come from the internal register (Burst Write Address register), which increments with each access.

SEARCH Instructions

Full Word Searches

In the first cycle of full word searches, the host will drive the OPV high and apply the instruction on OP[8:0]. For the SEARCH operation, OP[5:3] carries the index to the Global Mask register, whereas OP[8:6] carries the address to be matched on SADR[21:19]. DQ[67:0] will then transport the data to compare with the CAM array's [135:68] field.

In the second cycle, the host drives the OPV high and applies the instruction to OP[8:0], whereas OP[5:2] transports the index to the Comparand registers and then sends the full, 136-bit, word (which was presented during the first and second cycles) to the DQ bus. The OP[8:6] carries the index to the Result register to store the matching index and the match valid flag, whereas DQ[67:0] carries the data to be compared with CAM array bits 0 through 67. The resultant of the SEARCH instruction will then appear as a pipelined, SRAM READ cycle.

The pipelined SEARCH instruction completes in two clock cycles. All SRAM interface signals, MV, MF, and /MM shift to the right for different values of TLSZ. Additionally, MV, MF, and /MM shift to the right for different values of RLAT. See Tables 24 and 25 for the TLSZ and RLAT shift values.

Note: The word in use must have bit 0 set to one, whereas an empty word must have bit 0 set to 0.

Half-Word Searches

In the first cycle of half-word searches, the host drives the OPV high and applies the instruction to OP[8:0]. For the SEARCH instruction, the OP[5:3] carries the index to the Global Mask register, whereas OP[8:6] carries the address to be matched on SADR[21:19]. The DQ[67:0] will then transport the data to be compared with the CAM array's [67:0] field.

In the second cycle, the host drives the OPV high and applies the instruction to the OP[8:0] field. The OP[5:2] transports the index to the Comparand registers to be stored, and then sends the half, 68-bit word (which was presented during the first and second cycles) to the DQ bus. The OP[8:6] will transport the index to the Result register to store the match index and the match valid flag. The full word SEARCH instruction completes in four clock cycles after an initial latency search of four clock cycles; however, since the instruction is pipelined, searches can be performed every two cycles.

All SRAM interface signals, MV, MF, and /MM will shift to the right for different values of TLSZ. Additionally, MV, MF, and /MM shift to the right for different values of RLAT. See Tables 24 and 25 for the TLSZ and RLAT shift values.

Note: In the 68-bit configuration, the host must supply the same data on DQ[67:0] during the first and second cycles.

Double-Word Searches

The double word SEARCH instruction completes in four clock cycles after an initial latency search of four clock cycles; however, since the instruction is pipelined, searches can be performed every two cycles.

In the first cycle, the host drives the OPV to high and applies the instruction on OP[8:0]. In this cycle OP[2] must be set to 1. OP[5:3] carries the Global Mask register index to be applied to field [271:136] of the search data whereas DQ[67:0] carries the data to be compared with the CAM array's field of [271:204].

In the second cycle, the host also drives the OPV to high and applies the instruction on OP[8:0], whereas DQ[67:0] carries the data to be compared with the CAM array's field of [203:136].

In the third cycle, the host continues to drive the OPV to high and to apply the instruction on OP[8:0]. In this cycle OP[2] must be set to 0. OP[5:3] carries the Global Mask register index to be applied to field [135:0] of the search data. OP[8:6] carries the address to be supplied on SADR[21:19] if the device has a successful match. The DQ[67:0] carries the data to be compared with the [135:68] field of the CAM array.

In the fourth cycle, the host continues to drive OPV high and apply the instruction on OP[8:0]. The DQ[67:0] carries the data to be compared against the [67:0] field of the CAM array.

In the 272-bit configuration, the SEARCH instruction will be completed in four clock cycles. The SEARCH instruction results appear as a pipelined SRAM READ cycle with its latency measured from the second cycle of the instruction.

For all SRAM interface signals, MV and MF will shift to the right for different values of TLSZ. Additionally, MV, MF, and /MM shift to the right for different values of RLAT. See Tables 24 and 25 for the TLSZ and RLAT shift values.

Write Next Free Address

The WRITE NEXT FREE ADDRESS instruction can be completed in two clock cycles; the following delineates the instruction sequence.

In the first half of the first cycle, the host applies the WRITE NEXT FREE ADDRESS instruction on OP[1:0] and sets the instruction data valid to one (OPV = 1). OP[5:2] specifies the index of the even and odd comparand registers that will be written in the 136-bit configuration. In the 68-bit configuration, the even numbered comparands are specified by this index. OP[8:6] transports the bits to be driven on SADR[21:19] during the SRAM WRITE. In the second half of the first cycle, the host continues to drive OPV to 1, OP[1:0] to 11, and OP[5:2] with the even and odd comparand indexes. OP[6] equals 0 for a half-word searches of the next free address, and equals one for full word searches of the next free address.

In the second cycle, the host will set the instruction data valid signal to 0 (OPV = 0). After the completion of the second cycle, the CAM is ready for the next instruction. The search latency of the SRAM WRITE instruction is the same as the search latency to the SRAM READ instruction; it is measured from the second cycle of the WRITE NEXT FREE ADDRESS instruction.

When the host applies the WRITE NEXT FREE ADDRESS instruction specifying the appropriate comparand register, Harmony writes the specified comparand in the next free location in the depth-cascaded table. The next free location is the first entry in a Harmony with its bit [0] set to 0. If all the entries within the first Harmony are occupied (bit[0] = 1), then the first entry with bit[0] = 0 in a downstream Harmony in a group of cascaded devices is the next free location. In 136-bit configuration, bit[0] of both the even and the odd locations are both 0 when empty or both 1 when filled.

When configured for depth cascading, the FF signal indicates to the host when no more entries can be written, and when all entries within a group of cascaded devices are occupied. Harmony updates the signal to the CAM array after each WRITE or WRITE NEXT FREE ADDRESS instruction.

When configured for full words, the WRITE NEXT FREE ADDRESS instruction writes to both the even and odd Comparand registers in the data locations and uses the Next Free Address register as the address. It generates a WRITE to the external SRAM and also uses the Next Free Address register as a portion of the SRAM address.

When configured for half-words, the WRITE NEXT FREE ADDRESS instruction writes only to the even comparand register within the data location and uses the NFA register as the address. It generates a WRITE to the external SRAM and also uses the Next Free Address register as a portion of the SRAM address. The WRITE NEXT FREE ADDRESS

instruction only supports 68 or 136 words and does not support multiple search tables of different widths in depth cascaded configurations. In others words, all tables must be single, equal width tables.

SRAM Addressing

Index[13:0] (for 1M Harmony) and Index[14:0] (for 2M Harmony) contains the address, of a half-word entries, that results in a successful match; when configured, it is this address that resides on the full and double-word page boundaries, respectively.

SADR[13:0] (for 1M Harmony) and SADR[14:0] (for 2M Harmony) contains the address supplied on the DQ bus during device READ or WRITE accesses. See Tables 22 and 23 for the SRAM addressing.

SRAM READ or WRITE Accesses

SRAM READ

The SRAM READ enables and accesses associative data contained in external SRAM. An SRAM READ instruction completes in six cycles and the following delineates the instruction sequence.

In the first cycle, the host applies the READ instruction on OP[1:0], and sets the instruction data valid to one (OPV = 1). The DQ bus then supplies the appropriate address, sets DQ[20:19] to 10, and selects the SRAM address. The host selects the device for which the UID[4:0] matches DQ[25:21] and supplies SADR[21:19] to OP[8:6]. In the second and third cycles, the host 3-states DQ[67:0].

In the fourth cycle, the selected device starts to drive DQ[67:0] and drives the acknowledge signal, /ACK, from HIGHZ to low. In the fifth cycle, the selected device drives the READ address on SADR[21:0]; it also drives /ACK high, /CE low, and /ALE low. In the sixth cycle, the selected device 3-states /CE, SADR, and the DQ bus and continues to drive /ACK low. At the end of sixth cycle, the selected device 3-states /ACK.

SADR[13:0] contains the address supplied on the DQ bus during access to Harmony. Furthermore, OP[8:6] transports signals from the instruction bus to the SRAM[21:19] address bus.

SRAM WRITE

The SRAM WRITE instruction enables and writes associative data contained in external SRAM. An SRAM WRITE instruction completes in three clock cycles on the DQ bus.

In the first cycle, the host ASIC applies the WRITE instruction on CMD[1:0] (with CMD[2] = 0), and sets the command valid signal to one (CMDV = 1). The DQ bus then supplies the SRAM address, sets DQ[20:19] to 10. The host ASIC selects the device for which the UID[4:0] matches DQ[25:21]; it selects the device with LCAM bit set when DQ[25:21] = 11111. In the second and third are necessary wait cycles.

Table 22: SRAM Addressing for 1M Harmony

Instruction	SRAM Operation	21	20	19	18	[17:14]	[13:0]
SEARCH	Read	C8	C7	C6	1	UID[3:0]	Index[13:0]
WRITE NEXT FREE ADDRESS	Write	C8	C7	C6	1	UID[3:0]	NFA[13:0]
READ	Read	C8	C7	C6	1	UID[3:0]	SADR[13:0]
WRITE	Write	C8	C7	C6	1	UID[3:0]	SADR[13:0]
Indirect Access	Write/Read	C8	C7	C6	1	UID[3:0]	RR[13:0]

Table 23: SRAM Addressing for 2M Harmony

Instruction	SRAM Operation	21	20	19	[18:15]	[14:0]
SEARCH	Read	C8	C7	1	UID[3:0]	Index[14:0]
WRITE NEXT FREE ADDRESS	Write	C8	C7	1	UID[3:0]	NFA[14:0]
READ	Read	C8	C7	1	UID[3:0]	SADR[14:0]
WRITE	Write	C8	C7	1	UID[3:0]	SADR[14:0]
Indirect Access	Write/Read	C8	C7	1	UID[3:0]	RR[14:0]

Table 24: Right-Shift of Signals for TLSZ Values

TLSZ	Number of CLK Cycles	Number of Devices
00	0	1
01	1	2 - 8
10	2	5 - 8

Table 25: Right-Shift of Signals for RLAT Values

RLAT	Number of CLK Cycles
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

APPLICATION INFORMATION

34-Bit Word Applications

Some applications (e.g. IPv4, IPv4 CIDR, MPLS and ATM entries) will warrant smaller content addressable widths, such as 34-bit one-quarter words. For IPv4 (non-CIDR), MPLS and ATM addresses, a one-cycle technique that is not fully associative can be used. To ensure that table look-ups are completed in one-cycle, the designer must determine which of the entries are stored in the high quarter-word (bits 34 through 67) or low quarter-word (bits 0 through 33) based upon a single bit of the value to be stored (e.g., bit 0 of the network address). Based upon the value of the selected address bit to be found, while performing search operations, the Global Mask register can be used to restrict the search to the high or low quadrant of the 68-bit half-word.

Hence, the rationale is to perform two search operations of Harmony's content addressable array, where the first search will be performed on the bits 0 through 33 with the Mask register configured as zeroes, or "don't cares" in bits 34 through 67. The second search will be performed upon bits 34 through 67 while bits 0 through 33 will be masked out using the Global Mask register.

Harmony can perform both 68-bit and 136-bit fully associative searches in a single clock cycle. However, for 34-bit searches (with two 34-bit entries per 68-bit word), the designer must decide between one-cycle searches, which are not fully associative, or two-cycle searches that are fully associative. Where the above approach is unacceptable, or when IPv4 using CIDR addresses, two alternatives are available that provide fully associative searches. The first alternative simply stores single 34-bit entries into each 68-bit half-word. This ensures that searches are completed in one-cycle at the expense of less efficient memory utilization. The second alternative performs two linear search operations: one on the high order and the other on the low order 34-bits. This second approach provides more efficient memory utilization at the expense of reduced search speeds.

Hence, 32-bit data must be entered in two iterations, masking out the bits of the right side then the left side of the device. Since the search operations must be performed twice, thus, decreasing the speed to 50 million searches per second instead of the usual 100 million searches per second for the 68-bit and 136-bit configurations. Furthermore, in the case where a match may be produced on both halves of Harmony, the desired information of the left half has the higher priority. For example, if a successful match is found within the left half then the right half will not be searched. Hence, information must be written on the left half first then the right half.

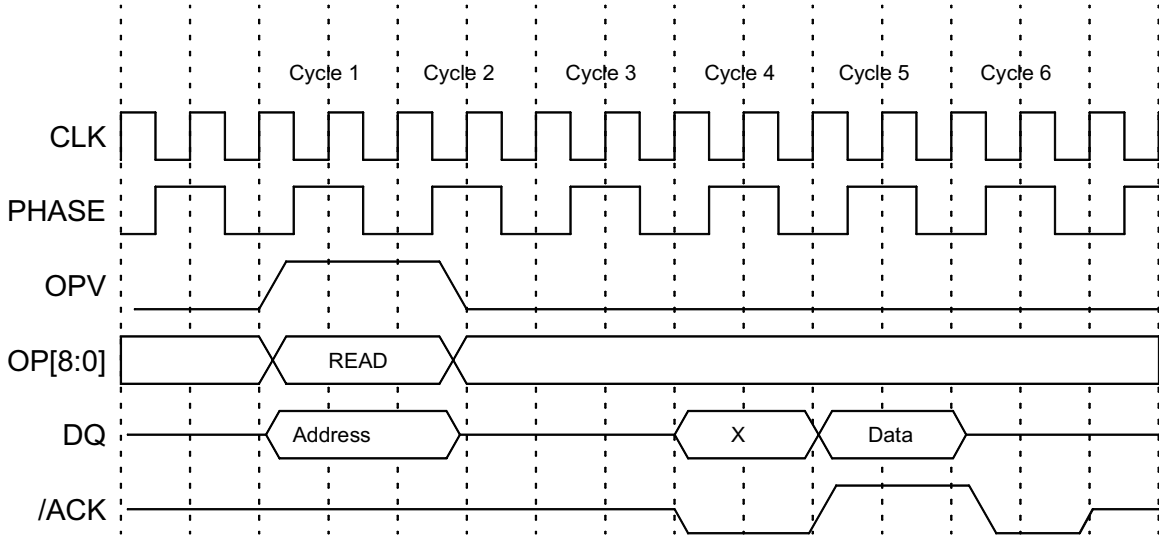# TIMING DIAGRAMS

Single Location Read Timing Diagram

Figure 11: Single Location Read Timing Diagram
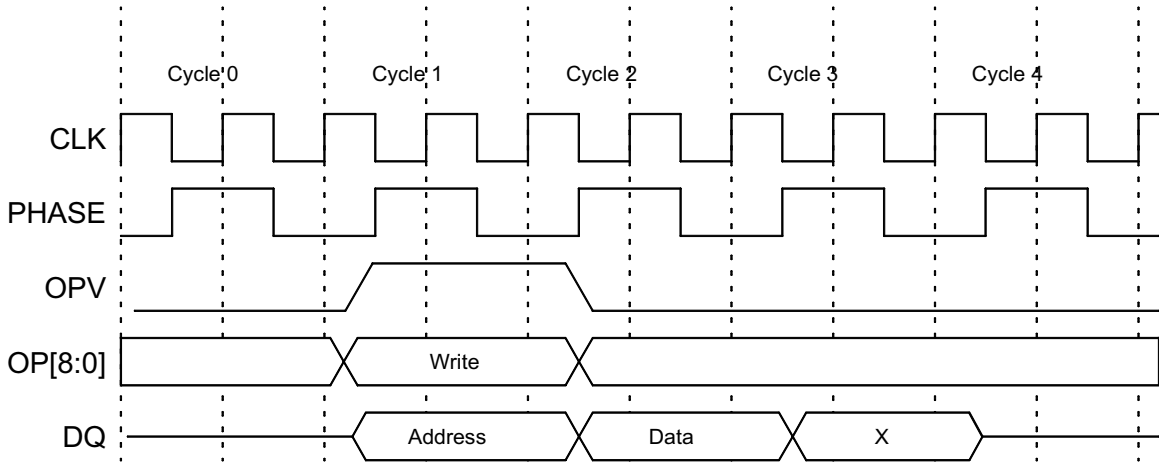
Write Cycle Timing Diagram

Figure 12: Write Cycle Timing Diagram

Data and Mask READ (BLEN = 4) for a Group of Cascaded Devices Timing Diagram
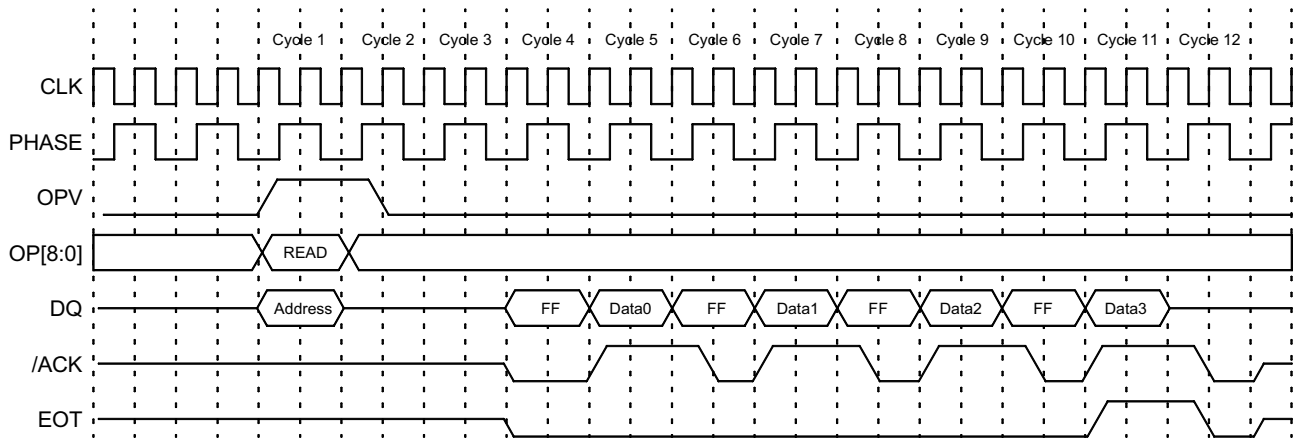
Figure 13: Data and Mask READ (BLEN = 4) for a Group of Cascaded Devices Timing Diagram

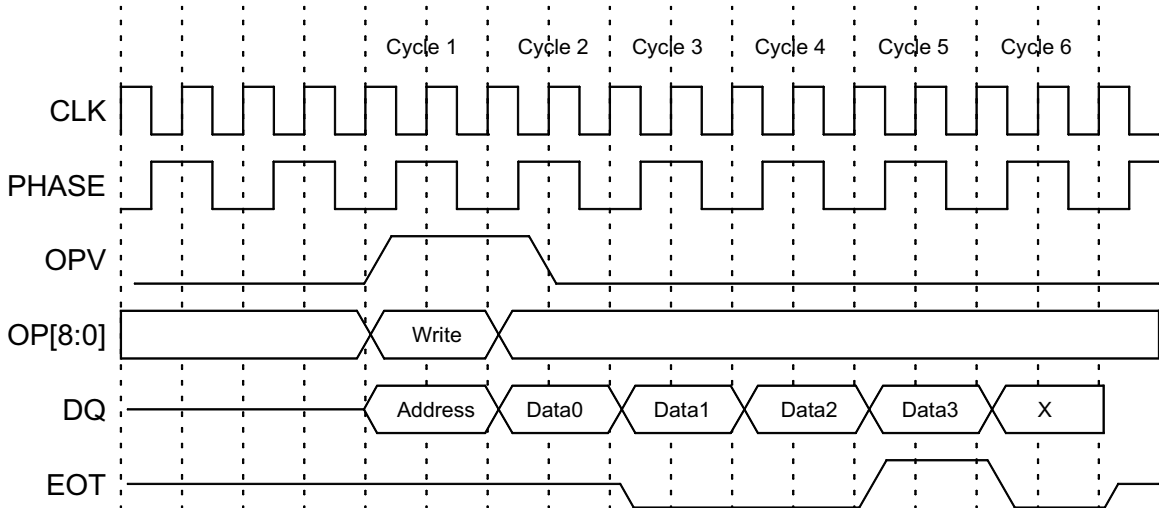## Data and Mask WRITE (BLEN = 4) for a Group of Cascaded Devices Timing Diagram

Figure 14: Data and Mask WRITE (BLEN = 4) for a Group of Cascaded Devices Timing Diagram

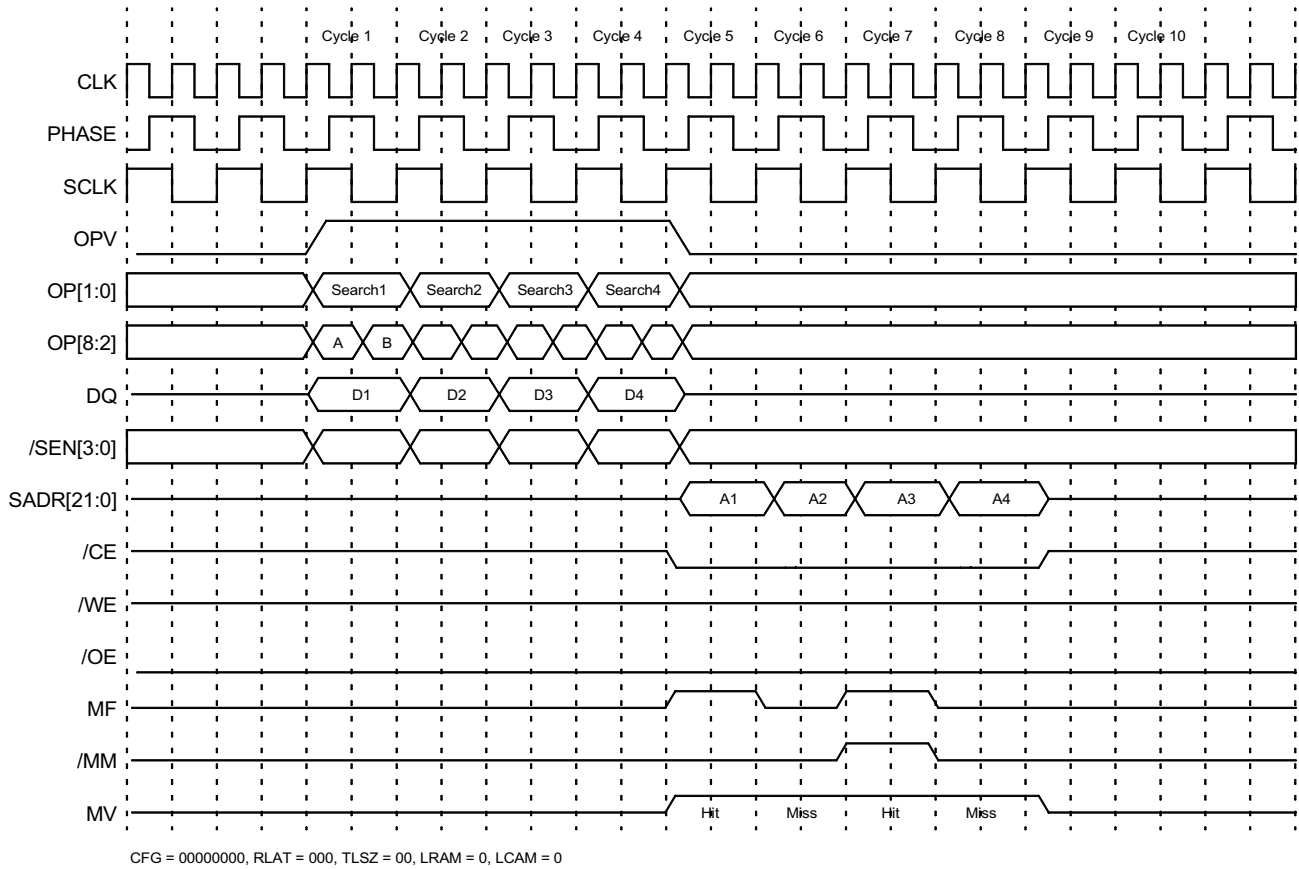## 68-Bit SEARCH Operation Timing Diagram

Figure 15: 68-Bit SEARCH Operation Timing Diagram
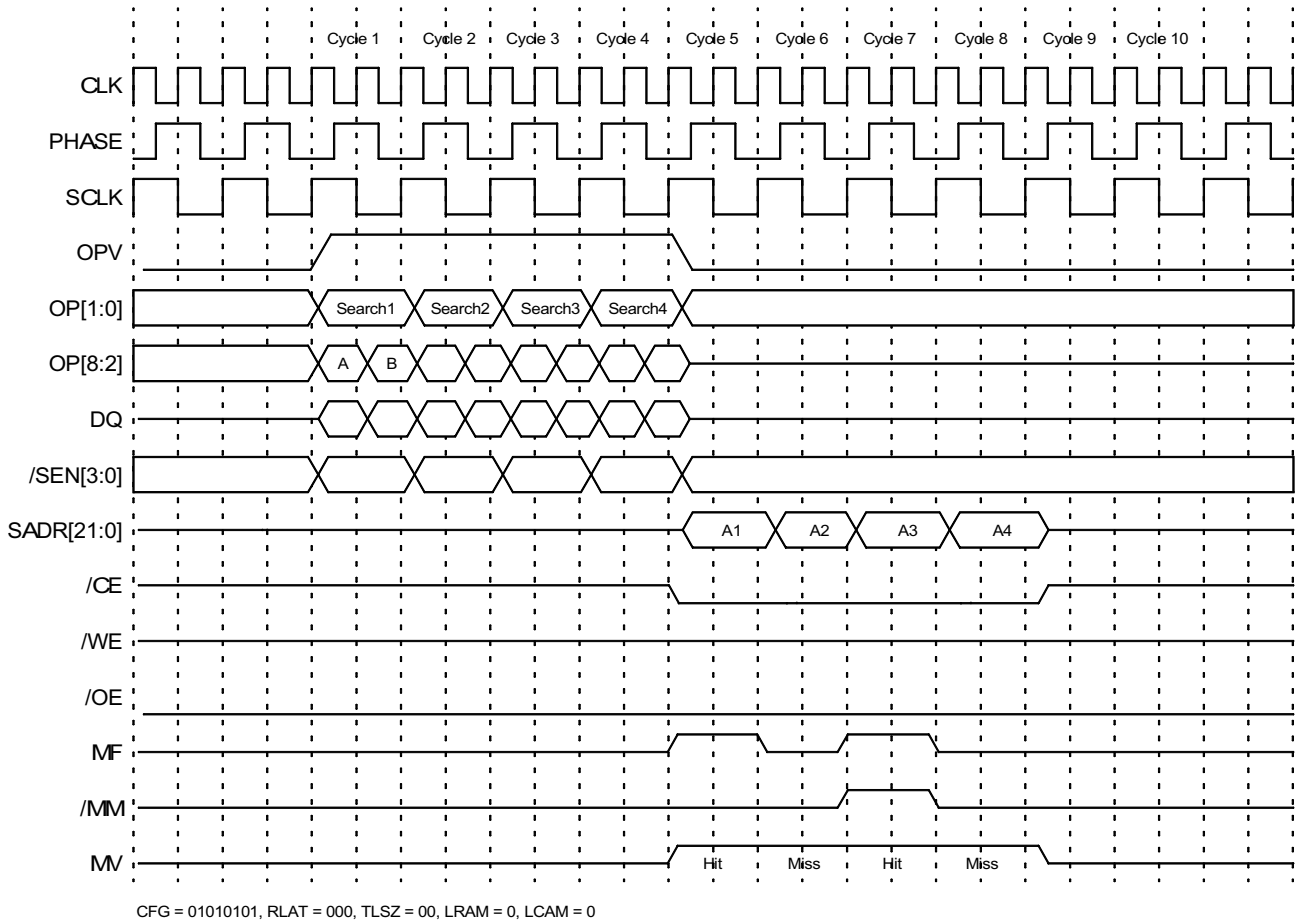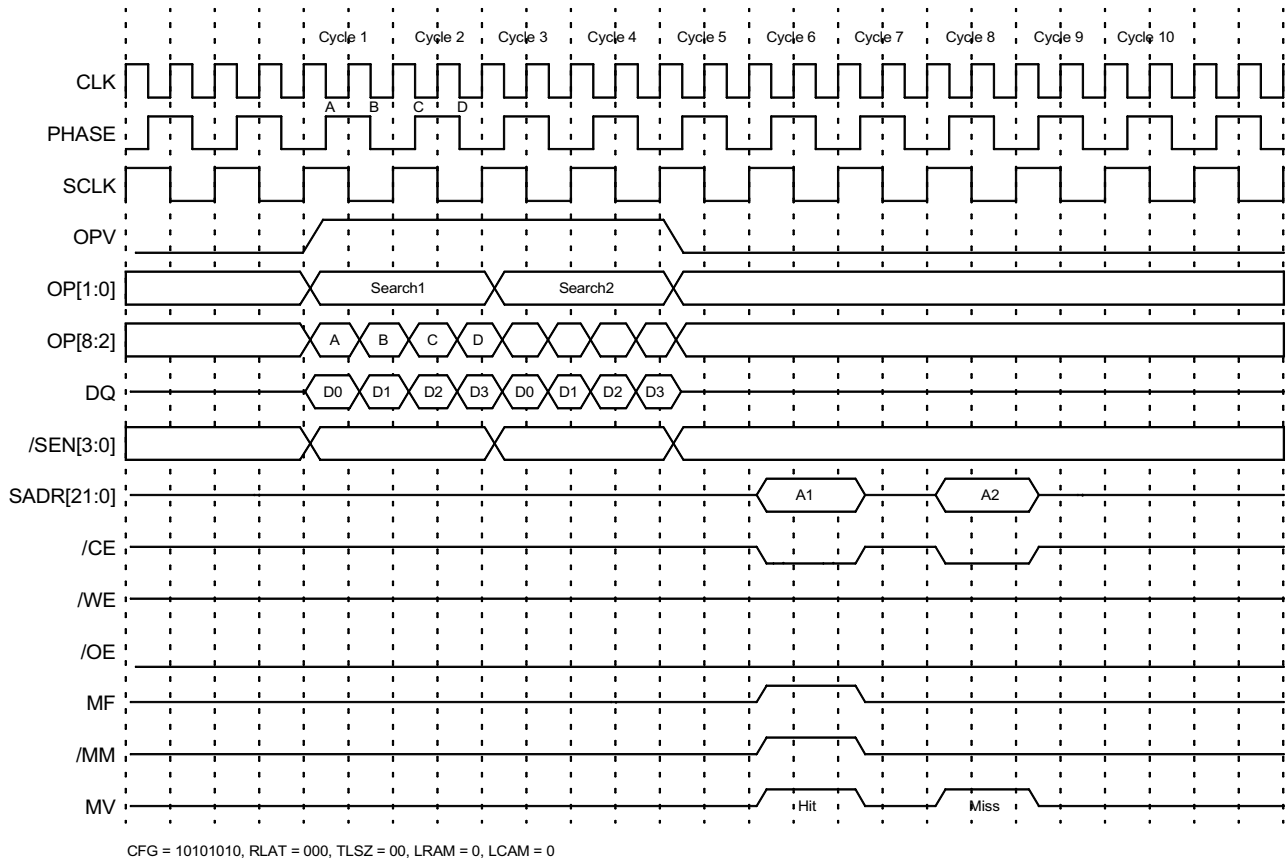
136-Bit SEARCH Operation Timing Diagram

CFG = 01010101, RLAT = 000, TLSZ = 00, LRAM = 0, LCAM = 0

Figure 16: 136-Bit SEARCH Operation Timing Diagram

272-Bit SEARCH Operation Timing Diagram

CFG = 10101010, RLAT = 000, TLSZ = 00, LRAM = 0, LCAM = 0

Figure 17: 272-Bit SEARCH Operation Timing Diagram

Arbitration for a Group of Cascaded Devices Timing Diagram

RLAT = 000, TLSZ = 01, LRAM = 0, LCAM = 0
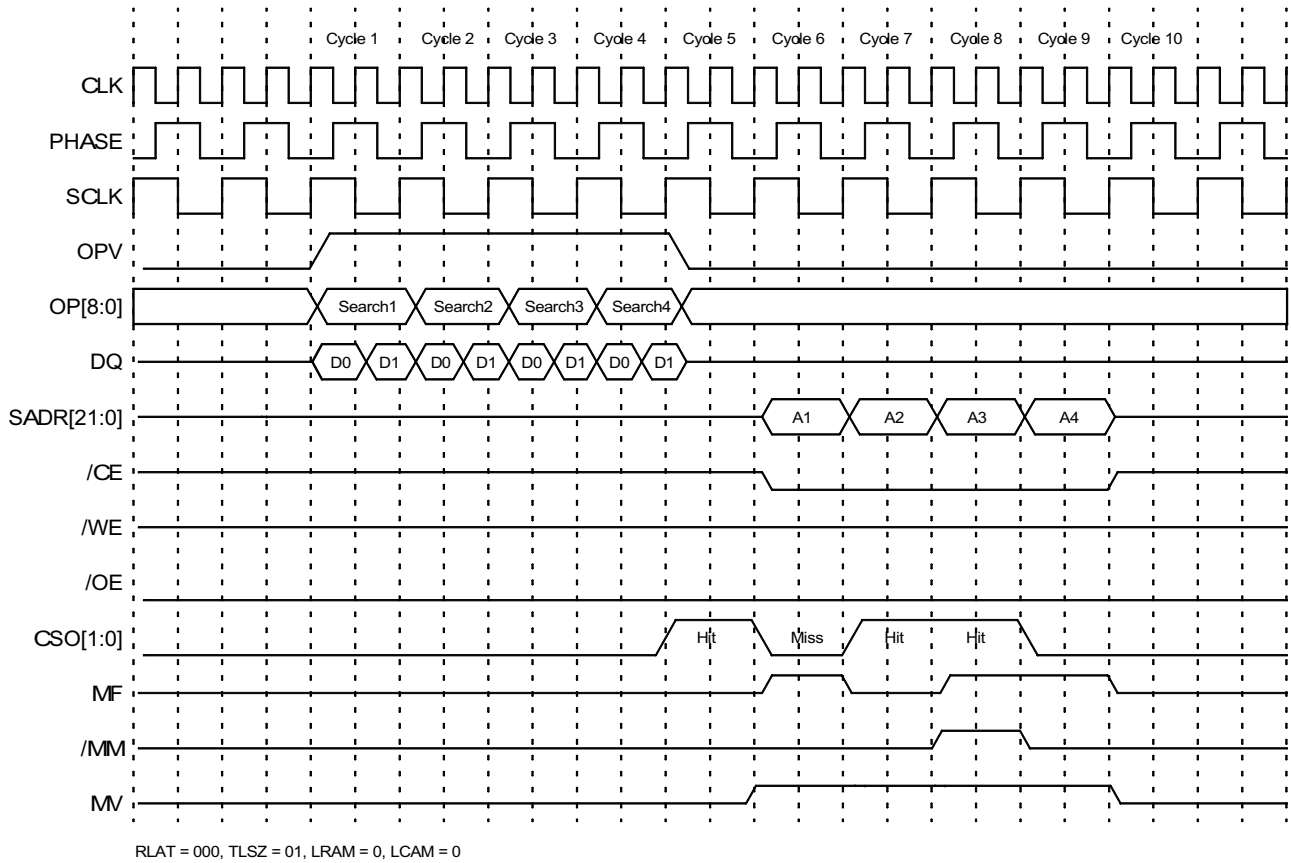
Figure 18: Arbitration for a Group of Cascaded Devices Timing Diagram

WRITE Timing Diagram

TLSZ = 00, LRAM = 0
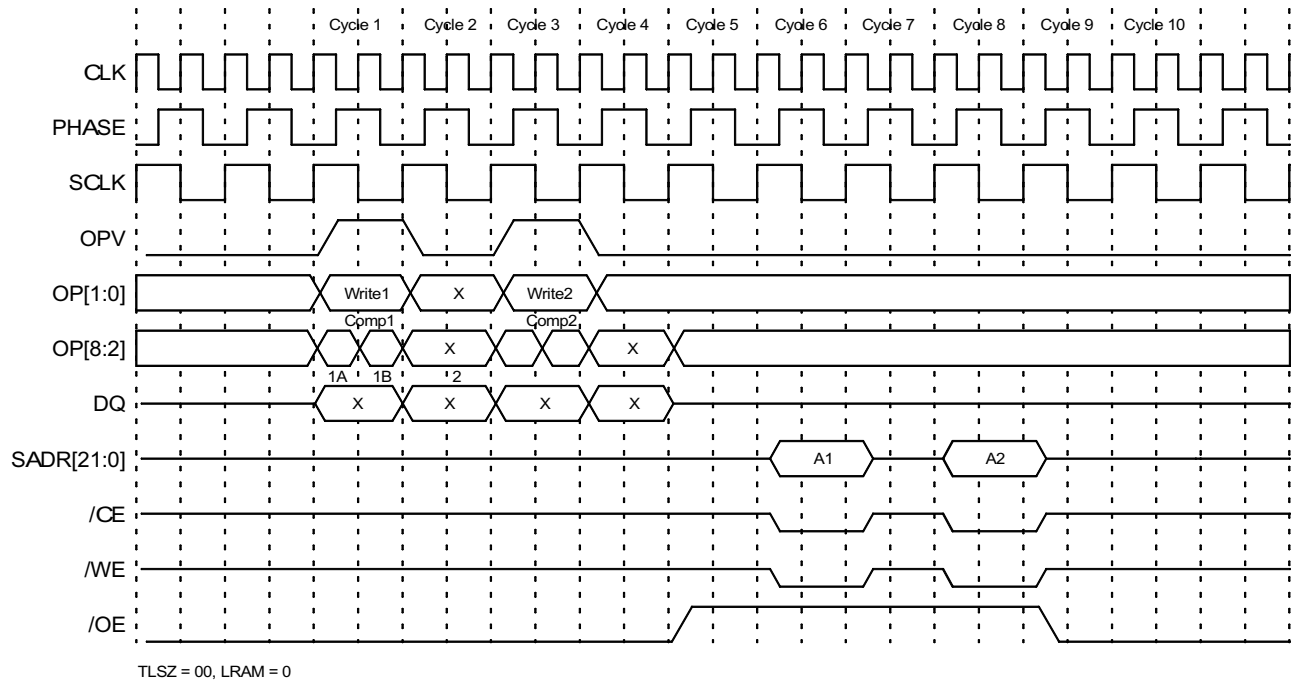
Figure 19: WRITE Timing Diagram

SRAM READ Cycle Timing Diagram

RLAT = 000, TLSZ = 00, LRAM = 0, LCAM = 0
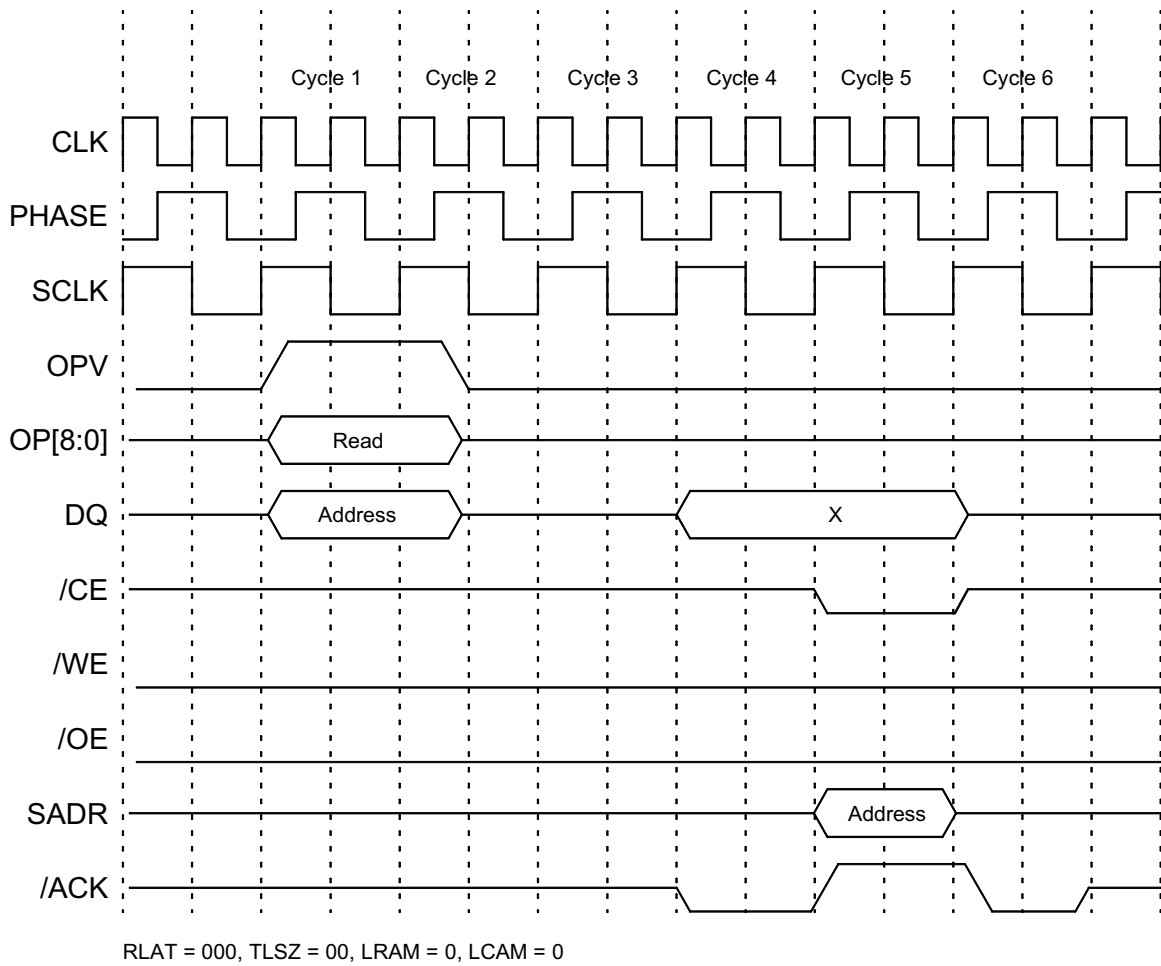
Figure 20: SRAM READ Cycle Timing Diagram

SRAM WRITE Cycle TIming Diagram

RLAT = 000, TLSZ = 00, LTAM = 0, LCAM = 0
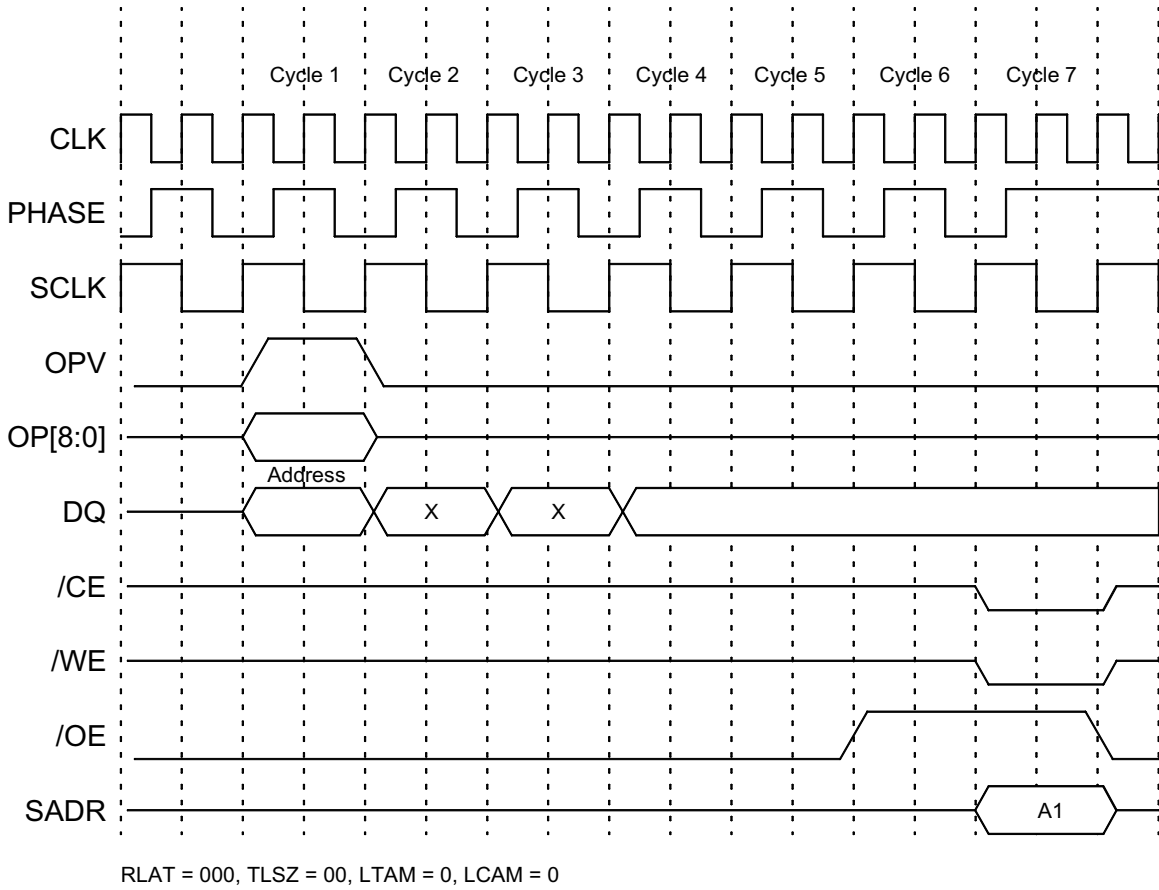
Figure 21: SRAM WRITE Cycle Timing Diagram

AC Timing Waveforms

Signal Group 1: PHASE, OP[8:0], OPV, /RST
SIgnal Group 2: CSI[6:0], FI[6:0]
Signal Group 3: CSO[1:0], FO[1:0], FF, MF, /MM, MV, /SEN[3:0]
Signal Group 4: /CE, /OE, /WE, /ALE
Signal Group 5: DQ, /ACK, EOT
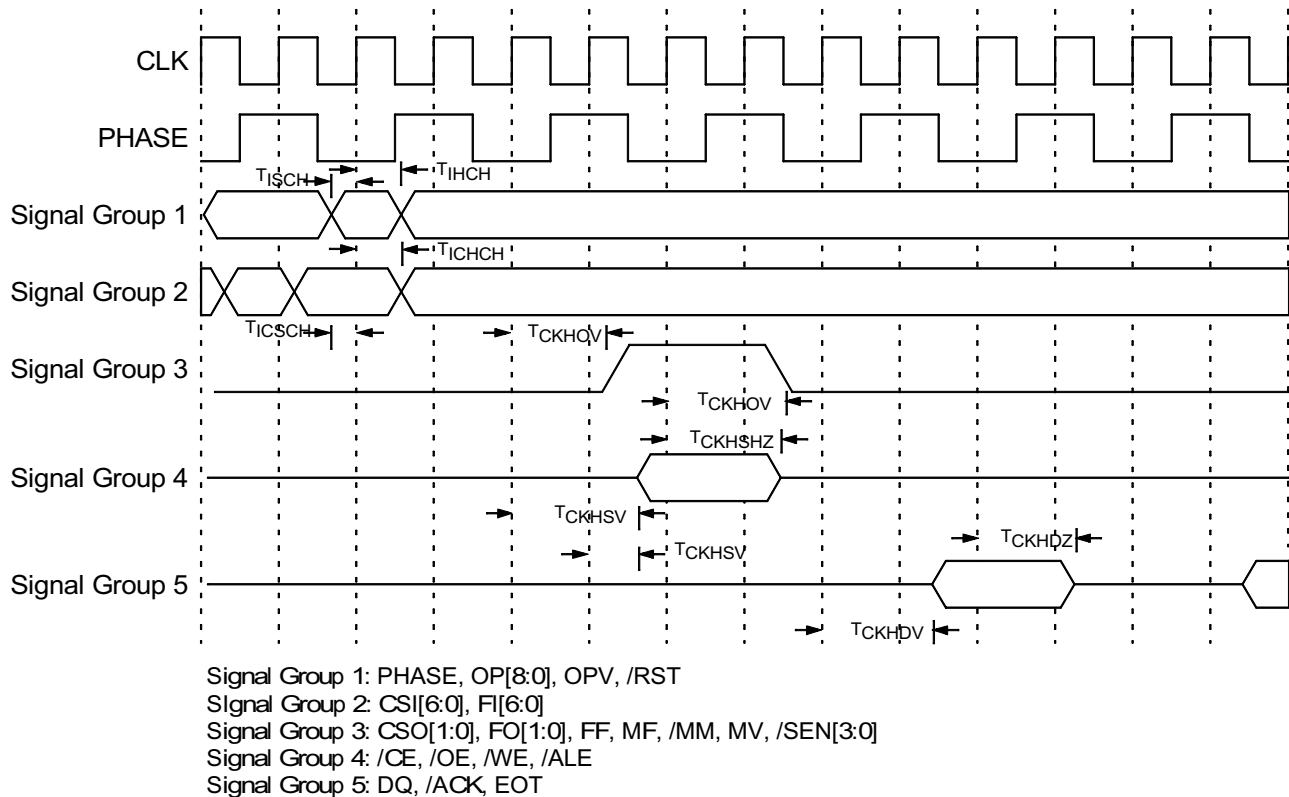
Figure 22: AC Timing Waveforms

Table 26: AC Timing Parameters

Row	Symbol	-66		-83		-100		Unit	Description
		Min	Max	Min	Max	Min	Max		
1	T_{CLK}		133		166			MHz	CLK2X period; Max frequency
2	T_{CKHI}	2.9		2.4				ns	CLK2X high pulse; worst-case 40%/60% duty cycle[1]
3	T_{CKLO}	2.9		2.4				ns	CLK2X low pulse; worst-case 40%/60% duty cycle[1]
4	T_{ISCH}	1.8		1.5				ns	Input Setup Time to CLK2X rising edge
5	T_{IHCH}	0.6		0.5				ns	Input Hold Time to CLK2X rising edge
6	T_{ICSCH}	4.2		3.5				ns	Cascaded Input Setup Time to CLK2X rising edge
7	T_{ICHCH}	0.6		0.5				ns	Cascaded Input Hold Time to CLK2X rising edge
8	T_{CKHOV}		10.2		8.5			ns	Rising edge of CLK2X to LHO, FULO, BHO, FULL valid[2]
9	T_{CKHDV}		11.4		9.5			ns	Rising edge of CLK2X to DQ valid[3]
10	T_{CKHDZ}	1.2	8.4	1.0	7.0			ns	Rising edge of CLK2X to DQ 3-state[4, 5]
11	T_{CKHSV}	3.6	11.4	3.0	9.5			ns	Rising edge of CLK2X to SRAM bus valid[3]
12	T_{CKHSHZ}		3.6		3.0			ns	Rising edge of CLK2X to SRAM bus HIGHZ[4, 5]
13	T_{CKHSLZ}		3.6		3.0			ns	Rising edge of CLK2X to SRAM bus LOWZ[4, 5]

Notes:

1. *TCLKHI and TCKLO duty cycle values are based on 20-80% signals levels.*

2. *Based on an AC load of 30 pF.*

3. *Except on notes cases, all values are based on AC load 50 pF measured at 1.5 V reference levels.*

4. *Based on AC load of 10 pF, 50-W DC loading and measured at 200mV from steady state.*

5. *These parameters are sampled and not 100% tested.*

ELECTRICAL SPECIFICATIONS

This section describes the electrical specifications, capacitance, operating conditions, and DC characteristics for the Harmony devices.

Electrical Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{DDQ}$	-10	10	µA
I_{LO}	Output Leakage Current[1]	$0 \le V_{OUT} \le V_{DDQ}$	-10	10	µA
V_{OL}	Output Low Voltage	8mA, V_{DDQ} = 3.3V		0.4	V
V_{OH}	Output High Voltage	4mA, V_{DDQ} = 3.3V	2.4		V
I_{DD}	1.8 V Supply Current[2]			TBD	mA
I_{DDQ}	3.3 V Supply Current[2]			TBD	mA

1.   *Applies only for outputs in 3-state.*
2.   *Average operating current at maximum frequency. Transient peak currents may exceed these values.*

Capacitance

Symbol	Parameter	Max	Unit
C_{IN}	Input Capacitance	6	pF[1]
C_{OUT}	Output Capacitance	6	pF[2]

1.   *$f = 1\ MHz$, $V_{IN} = 0\ V$*

2.   *$f = 1\ MHz$, $V_{OUT} = 0\ V$*

Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{DDQ}	Operating Voltage for IO	3.0	3.6	V
V_{DD}	Operating Supply Voltage	1.65	1.95	V
V_{IH}	Input High Voltage[1]	2.0V	V_{DDQ}+0.3	V
V_{IL}	Input Low Voltage[2]	-0.3	0.8	V
T_A	Ambient Operating Temperature	0	70	ºC
	Supply Voltage Tolerance	-10%	+10%	

Notes:

1.   *Maximum allowable applies to overshoot only (V_{DDQ} is 3.3 V supply).*

2.   *Minimum allowable applies to undershoot only.*

PACKAGE
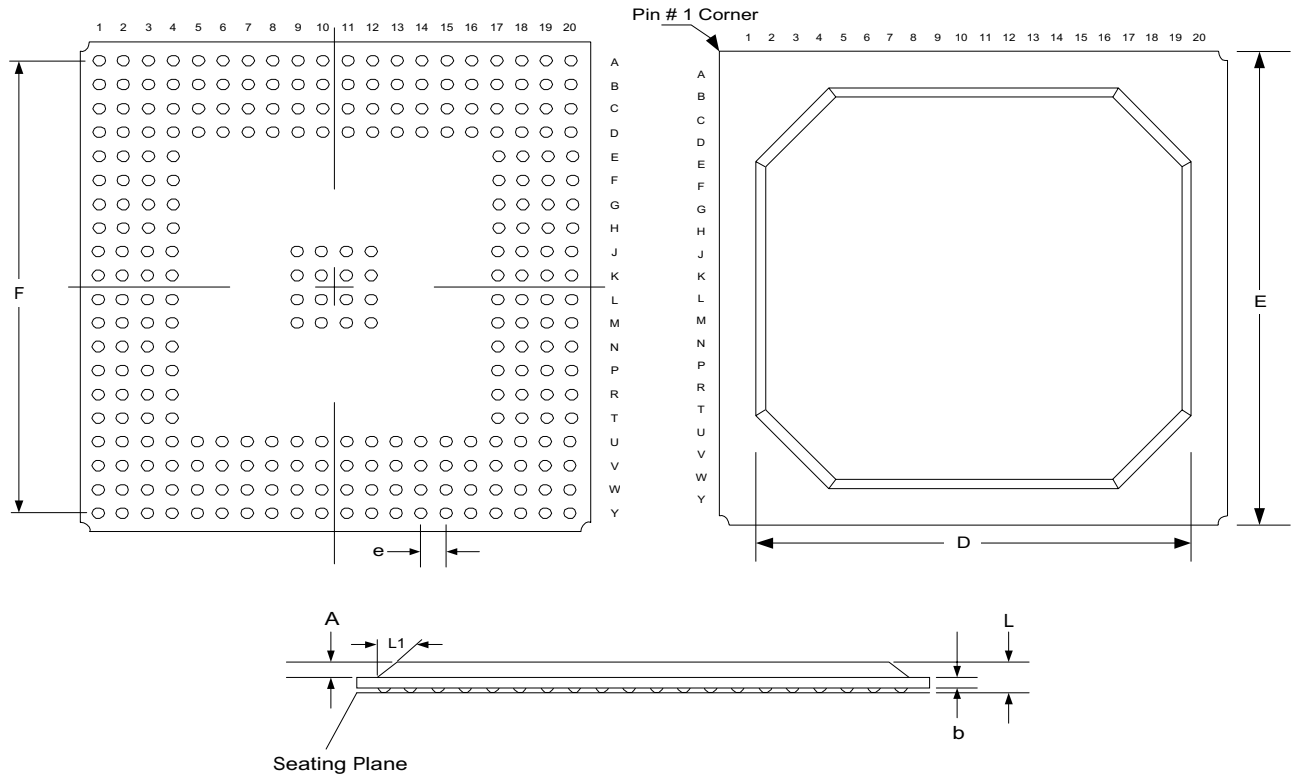
272-Pin BGA Dimensions

	Dim. A	Dim. b	Dim. D	Dim. E	Dim. e	Dim. F	Dim. L	L1
Min.				26.80			0.50	
Nom.	1.17	0.04	24.00	27.00	1.27	24.13	0.60	30° TYP.
Max.				27.20			0.70	

ORDERING

Part Number	Density	Clock Speed	Package	Temperature	Voltage
MUAD16K136-66B272C	2Mbit	66 MHz	272-Pin BGA	0 - 70°	1.8/3.3V
MUAD16K136-83B272C		83 MHz	272-Pin BGA	0 - 70°	1.8/3.3V
MUAD16K136-10B272C		100 MHz	272-Pin BGA	0 - 70°	1.8/3.3V
MUAD8K136-66B272C	1Mbit	66 MHz	272-Pin BGA	0 - 70°	1.8/3.3V
MUAD8K136-83B272C		83 MHz	272-Pin BGA	0 - 70°	1.8/3.3V
MUAD8K136-10B272C		100 MHz	272-Pin BGA	0 - 70°	1.8/3.3V

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